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=> file reg
FILE 'REGISTRY' ENTERED AT 12:12:03 ON 25 JUL 2003
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=> display history full l1-


     FILE 'REGISTRY' ENTERED AT 09:51:30 ON 25 JUL 2003
                E PTFE/CN
L1            1 SEA PTFE/CN
                D RN
                E TETRAFLUOROETHYLENE/CN
L2            1 SEA TETRAFLUOROETHYLENE/CN
                D RN
L3         3923 SEA 116-14-3/CRN
                E TRIFLUOROMETHYL VINYL ETHER/CN
L4            1 SEA "TRIFLUOROMETHYL VINYL ETHER"/CN
                D RN
L5           17 SEA 1645-89-2/CRN
L6           13 SEA L3 AND L5
L7            1 SEA L6 AND 2/NC
                E PERFLUOROETHYLENE/CN
L8            1 SEA PERFLUOROETHYLENE/CN
                D RN
L9         3923 SEA 116-14-3/CRN
                E PERFLUOROPROPYLENE/CN
L10           1 SEA PERFLUOROPROPYLENE/CN
                D RN
L11        1489 SEA 116-15-4/CRN
L12         504 SEA L9 AND L11
                E PROPYLENE/CN
L13           1 SEA PROPYLENE/CN
                D RN
L14        6016 SEA 115-07-1/CRN
L15         234 SEA L9 AND L14
L16           2 SEA L12 AND 2/NC
L17           4 SEA L15 AND 2/NC
                E ETHYLENE/CN
L18           1 SEA ETHYLENE/CN
                D RN
L19       12579 SEA 74-85-1/CRN
L20         451 SEA L19 AND L3
L21           4 SEA L20 AND 2/NC
                E CHLOROTRIFLUOROETHENE HOMOPOLYMER/CN
L22           1 SEA "CHLOROTRIFLUOROETHENE HOMOPOLYMER"/CN
                E CHLOROTRIFLUOROETHENE/CN
L23           1 SEA CHLOROTRIFLUOROETHENE/CN
                D RN
L24        3162 SEA 79-38-9/CRN
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L25           138 SEA L24 AND L19
L26             3 SEA L25 AND 2/NC
                  E VINYLIDENE DIFLUORIDE HOMOPOLYMER/CN
L27             1 SEA "VINYLIDENE FLUORIDE HOMOPOLYMER"/CN
                  E VINYL FLUORIDE HOMOPOLYMER/CN
L28             1 SEA "VINYL FLUORIDE HOMOPOLYMER"/CN
                  E PERFLUORODIOXOL/CN
                  E FLUORODIOXOL/CN

     FILE 'LCA' ENTERED AT 10:20:17 ON 25 JUL 2003
L29             0 SEA ?PERFLUORODIOXOL?

     FILE 'HCA' ENTERED AT 10:20:22 ON 25 JUL 2003
L30            39 SEA ?PERFLUORODIOXOL?
L31             5 SEA ?POLYPERFLUORODIOXOL?
                  D L31 1-5 KWIC
                  D L31 5 ALL

     FILE 'REGISTRY' ENTERED AT 10:24:28 ON 25 JUL 2003
                  E PERFLUORODIOXOLANE/CN
                  E ?FLUORODIOXOL?/CNS
L32             0 SEA ?FLUORODIOXOL?/CNS

     FILE 'HCA' ENTERED AT 10:26:55 ON 25 JUL 2003
                  D L31 1-4 ALL
                  SEL L31

     FILE 'REGISTRY' ENTERED AT 10:29:01 ON 25 JUL 2003
L33        320618 SEA ?DIOXOL?/CNS
L34            94 SEA L33 AND L3
L35            40 SEA L34 AND 2/NC
L36            58 SEA L1 OR L7 OR L16 OR L17 OR L21 OR L22 OR L26 OR L27
                  OR L28 OR L35
                  SAV L36 CAM827/A

     FILE 'LCA' ENTERED AT 10:34:29 ON 25 JUL 2003
L37            73 SEA FLUOROPOLYM? OR PERFLUOROPOLYM? OR (FLUORINAT? OR
                  PERFLUORINAT? OR FLUORO OR PERFLUORO)(2A)(POLYM# OR
                  COPOLYM# OR HOMOPOLYM# OR TERPOLYM# OR POLYMER? OR
                  COPOLYMER? OR HOMOPOLYMER? OR TERPOLYMER? OR RESIN?)
L38            64 SEA (F OR FLUORINE#)(3A)(CONTAIN? OR CONTG#)(3A)(POLYM#
                  OR COPOLYM# OR HOMOPOLYM# OR TERPOLYM# OR POLYMER? OR
                  COPOLYMER? OR HOMOPOLYMER? OR TERPOLYMER? OR RESIN?) OR
                  FLUOROPOLYM? OR PERFLUOROPOLYM?

     FILE 'HCA' ENTERED AT 10:45:23 ON 25 JUL 2003
L39         55836 SEA L36
L40         64773 SEA L37 OR L38 OR FLUORORESIN? OR PERFLUORORESIN?

     FILE 'REGISTRY' ENTERED AT 10:45:35 ON 25 JUL 2003
                  E SILICON/CN
L41             1 SEA SILICON/CN
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     FILE 'LCA' ENTERED AT 10:46:01 ON 25 JUL 2003
L42        10451 SEA (SUBSTRAT? OR SURFACE? OR BASE# OR SUBSTRUCT? OR
                 UNDERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR PANE? OR
                 DISK? OR DISC# OR WAFER?)/BI,AB

     FILE 'HCA' ENTERED AT 10:48:19 ON 25 JUL 2003
L43       299598 SEA WAFER? OR DISK? OR DISC# OR (SILICON OR SI OR
                 L41)(2A)L42
L44       169461 SEA QUARTZ?
L45         5647 SEA L43(3A)(CARRIER? OR CARRY? OR CARRIED OR HOLD? OR
                 GRIP? OR GRASP? OR HANDL? OR BOAT? OR CHUCK? OR JIG OR
                 JIGS OR JIGGED OR JIGGING# OR FASTEN? OR AFFIX? OR
                 ATTACH?)
L46         2730 SEA (ROUND? OR BLUNT? OR DULL? OR UNSHARP? OR OBTUS? OR
                 OBTUND? OR RETUND? OR OBTUND? OR SMOOTH?)(2A)(EDGE# OR
                 EDGING# OR CORNER? OR RIM OR RIMS OR RIMMED OR RIMMING#
                 OR FLANG? OR ANGLE# OR VERTEX# OR VERTICE# OR APEX# OR
                 APICE#) OR UNEDG? OR DISEDG?
L47        16818 SEA (FLAME# OR FLAMING# OR FIRE# OR FIRING#)(2A)(TREAT?
                 OR PRETREAT? OR CONDITION? OR PRECONDITION? OR PROCESS?
                 OR PREPROCESS? OR POSTPROCESS?)
L48          228 SEA L43 AND L44 AND L45
L49            1 SEA L48 AND L47
L50            0 SEA L48 AND L46
L51      1275710 SEA CARRIER? OR CARRY? OR CARRIED OR HOLD? OR GRIP? OR
                 GRASP? OR HANDL? OR BOAT? OR CHUCK? OR JIG OR JIGS OR
                 JIGGED OR JIGGING# OR FASTEN? OR AFFIX? OR ATTACH?
L52          868 SEA L43 AND L44 AND L51
L53            2 SEA L52 AND L47
L54            2 SEA L52 AND L46
L55            0 SEA (L53 OR L54) AND (L39 OR L40)
L56           21 SEA L45 AND (L46 OR L47)
L57            1 SEA L56 AND L44
L58            0 SEA L56 AND (L39 OR L40)

     FILE 'HCAPLUS' ENTERED AT 11:13:00 ON 25 JUL 2003
L59          332 SEA INAKI ?/AU OR KYOICHI ?/AU
L60        11442 SEA ARAKI ?/AU OR ITSUO ?/AU
L61            2 SEA L59 AND L60

     FILE 'HCA' ENTERED AT 11:21:08 ON 25 JUL 2003
L62           18 SEA L43 AND L44 AND (L46 OR L47)
L63            4 SEA L62 AND (L51 OR L39 OR L40)
L64       211135 SEA (ETCH? OR PHOTOETCH? OR CHASE# OR CHASING# OR
                 ENCHAS? OR ENGRAV? OR PHOTOENGRAV? OR EMBOSS? OR
                 PHOTOEMBOSS? OR INCISE# OR INCISING# OR IMPRINT? OR
                 IMPRESS? OR ENCAUSTIC?)/BI,AB
L65            5 SEA L62 AND L64
                 E SEMICONDUCTOR DEVICE FABRICATION/CV
L66        39769 SEA "SEMICONDUCTOR DEVICE FABRICATION"/CV
                 E SILICON WAFER CLEANING/CV
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L67         75590 SEA (L41 OR SILICON OR SI)(2A)PROCESS?
L68           251 SEA (L66 OR L67) AND L44 AND L51
L69             2 SEA L68 AND (L46 OR L47)
L70             3 SEA L68 AND (L39 OR L40)
L71            47 SEA L68 AND L45
L72            12 SEA L71 AND L64
L73        965084 SEA CARRIER? OR CARRY? OR CARRIED OR HOLDER? OR GRIPER?
                  OR GRASPER? OR HANDLER? OR BOAT? OR CHUCK? OR JIG OR
                  JIGS OR JIGGED OR JIGGING#
L74          3821 SEA JIG OR JIGS OR JIGGED OR JIGGING#
L75            34 SEA L43 AND L44 AND L74
L76             1 SEA L75 AND (L46 OR L47)
L77             1 SEA L75 AND (L39 OR L40)
L78            12 SEA L75 AND (L66 OR L67)

     FILE 'HCA' ENTERED AT 11:44:50 ON 25 JUL 2003
L79             5 SEA L75 AND L64
L80           690 SEA L43 AND L44 AND L73
L81             4 SEA L80 AND (L46 OR L47)
L82             6 SEA L80 AND (L39 OR L40)
L83           100 SEA L80 AND L64
L84           108 SEA L80 AND (L66 OR L67)
L85            25 SEA L83 AND L84
L86            21 SEA L49 OR L53 OR L54 OR L57 OR L63 OR L65 OR L69 OR L70
                  OR L76 OR L77 OR L79 OR L81 OR L82
L87            30 SEA (L62 OR L72 OR L78) NOT L86
L88            13 SEA L85 NOT (L86 OR L87)

     FILE 'WPIDS, JAPIO' ENTERED AT 11:56:45 ON 25 JUL 2003
L89         37795 SEA QUARTZ#
L90         21592 SEA QUARTZ#
     TOTAL FOR ALL FILES
L91         59387 SEA QUARTZ#
L92         47998 SEA L43(3A)(CARRIER? OR CARRY? OR CARRIED OR HOLD? OR
                  GRIP? OR GRASP? OR HANDL? OR BOAT? OR CHUCK? OR JIG OR
                  JIGS OR JIGGED OR JIGGING# OR FASTEN? OR AFFIX? OR
                  ATTACH?)
L93         19944 SEA L43(3A)(CARRIER? OR CARRY? OR CARRIED OR HOLD? OR
                  GRIP? OR GRASP? OR HANDL? OR BOAT? OR CHUCK? OR JIG OR
                  JIGS OR JIGGED OR JIGGING# OR FASTEN? OR AFFIX? OR
                  ATTACH?)
     TOTAL FOR ALL FILES
L94         67942 SEA L45
L95         26769 SEA (ROUND? OR BLUNT? OR DULL? OR UNSHARP? OR OBTUS? OR
                  OBTUND? OR RETUND? OR OBTUND? OR SMOOTH?)(2A)(EDGE# OR
                  EDGING# OR CORNER? OR RIM OR RIMS OR RIMMED OR RIMMING#
                  OR FLANG? OR ANGLE# OR VERTEX# OR VERTICE# OR APEX# OR
                  APICE#) OR UNEDG? OR DISEDG?
L96          4789 SEA (ROUND? OR BLUNT? OR DULL? OR UNSHARP? OR OBTUS? OR
                  OBTUND? OR RETUND? OR OBTUND? OR SMOOTH?)(2A)(EDGE# OR
                  EDGING# OR CORNER? OR RIM OR RIMS OR RIMMED OR RIMMING#
                  OR FLANG? OR ANGLE# OR VERTEX# OR VERTICE# OR APEX# OR
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                APICE#) OR UNEDG? OR DISEDG?
     TOTAL FOR ALL FILES
L97         31558 SEA L46
L98          6880 SEA (FLAME# OR FLAMING# OR FIRE# OR FIRING#)(2A)(TREAT?
                OR PRETREAT? OR CONDITION? OR PRECONDITION? OR PROCESS?
                OR PREPROCESS? OR POSTPROCESS?)
L99          2658 SEA (FLAME# OR FLAMING# OR FIRE# OR FIRING#)(2A)(TREAT?
                OR PRETREAT? OR CONDITION? OR PRECONDITION? OR PROCESS?
                OR PREPROCESS? OR POSTPROCESS?)
     TOTAL FOR ALL FILES
L100         9538 SEA L47
L101            3 SEA L89 AND L92 AND (L95 OR L98 )
L102            0 SEA L90 AND L93 AND (L96 OR L99 )
     TOTAL FOR ALL FILES
L103            3 SEA L91 AND L94 AND (L97 OR L100)


=> file wpids
FILE 'WPIDS' ENTERED AT 12:12:18 ON 25 JUL 2003
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FILE LAST UPDATED:            23 JUL 2003      <20030723/UP>
MOST RECENT DERWENT UPDATE:       200347        <200347/DW>
DERWENT WORLD PATENTS INDEX SUBSCRIBER FILE, COVERS 1963 TO DATE


=> d l101 1-3 max

L101 ANSWER 1 OF 3  WPIDS  COPYRIGHT 2003 THOMSON DERWENT on STN
AN   2002-683955 [74]    WPIDS
DNN  N2002-539958       DNC C2002-193212
TI   Fluororesin-coated quartz glass jig e.g.
     wafer carrier boats for use in cleaning
     silicon wafers, has surface entirely covered with a pinhole-free
     fluororesin coating.
DC   A14 A88 L01 L03 P73 U11                         priority
IN   ARAKI, I; INAKI, K
PA   (HERA) HERAEUS QUARZGLAS GMBH & CO KG; (SHIN-N) SHINETSU QUARTZ PROD
     CO LTD; (SHIN-N) SHINETSU SEKIEI KK; (ARAK-I) ARAKI I; (INAK-I)
     INAKI K
CYC  28
PI   EP 1213269    A1 20020612 (200274)* EN    6p    C03C017-32
         R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK
            NL PT RO SE SI TR
     JP 2002176023 A  20020621 (200274)        4p    H01L021-304
     US 2002106518 A1 20020808 (200274)              B32B027-00
ADT  EP 1213269 A1 EP 2001-128581 20011130; JP 2002176023 A JP
     2000-369534 20001205; US 2002106518 A1 US 2001-6827 20011204
PRAI JP 2000-369534     20001205
IC   ICM  B32B027-00; C03C017-32; H01L021-304
AB   EP    1213269 A UPAB: 20021118
     NOVELTY - The entire surface of fluororesin-coated quartz
```

glass jig is covered with a pinhole free fluororesin coating.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for producing fluororesin-coated **quartz** glass jig, involves **rounding** all the **edges** of jig into curved portions each having a curvature (r) of 0.5 mm or more, and treating the resulting jig with fluororesin coating agent to form fluororesin coating on entire **quartz** glass jig.
USE - For e.g. **wafer carrier boats** and **chucks**, for use in cleaning silicon wafers.
ADVANTAGE - Since pinhole-free fluororesin is coated on entire surface of **quartz** glass jig, direct contact of **quartz** glass jig with hydrochloric acid solution is prevented. Thus, peeling of fluororesin coating or generation of particles during etching of **quartz** glass are prevented, while relaxing the impact on **quartz** glass imposed by silicon wafers, thereby preventing generation of chipping. The adhesiveness of fluororesin coating to **quartz** glass is improved by applying fluororesin solution having excellent heat resistance, chemical resistance, corrosion resistance and wear resistance, after subjecting **quartz** glass surface to frost treatment. By performing frost treatment, the irregularities are formed on surface of **quartz** glass and anchoring effect provided by the irregularities decreases peeling of film by improving adhesiveness of fluororesin coating. The silicon wafers are produced in high yield.
Dwg.0/0

TECH EP 1213269 A1 UPTX: 20021118
TECHNOLOGY FOCUS - POLYMERS - Preferred Composition: The fluororesin is tetrafluoroethylene resin, tetrafluoroethylene-perfluoroalkylvinyl ether resin, perfluoroethylene-propylene resin, ethylene-tetrafluoroethylene resin, chlorotrifluoroethylene resin, ethylene-chlorotrifluoroethylene resin, vinylidene difluoride resin, vinyl fluoride resin or tetrafluoroethylene-perfluorodioxol resin. Preferred Thickness: The thickness of fluororesin coating is 50 mum or more. Preferred Process: The fluororesin coating is formed on **quartz** glass jig after applying frost treatment to jig. The frost treatment is surface treatment performed using a chemical agent. The **rounding** of all **edges** of jig is carried out before frost treatment.

FS CPI EPI GMPI
FA AB
MC CPI: A04-E10; A12-H; L01-G04B; L04-C09; L04-D
EPI: U11-C06A1B; U11-F02A2
PLE UPA 20021118
[1.1] 018; P0500 F- 7A
[1.2] 018; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A; H0000; H0011-R; P0511
[1.3] 018; H0022 H0011; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A; R00976 G0022 D01 D12 D10 D51 D53 D59 D69 D83 F- 7A; P0544
[1.4] 018; H0022 H0011; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A; G0759 G0022 D01 D11 D10 D12 D51 D53 D59 D69 F34

F- 7A
[1.5] 018; H0022 H0011; R00326 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D82; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A; P1150; P0533
[1.6] 018; H0022 H0011; R00458 G0022 D01 D12 D10 D53 D51 D59 D69 D82 F- 7A Cl; R00326 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D82; P1150; P0522
[1.7] 018; R00339 G0544 G0022 D01 D12 D10 D51 D53 D58 D69 D82 F- 7A; R00363 G0555 G0022 D01 D12 D10 D51 D53 D58 D69 D82 F- 7A; H0000; H0011-R
[1.8] 018; H0022 H0011; G0806 G0022 D01 D51 D53 D23 D22 D31 D75 D46 D59 D69 D83 F24 F- 7A; R00975 G0022 D01 D12 D10 D51 D53 D59 D69 D82 F- 7A
[1.9] 018; ND01; Q9999 Q7114-R; Q9999 Q7921 Q7885; K9529 K9483; K9676-R; B9999 B5141 B4740; B9999 B5243-R B4740; N9999 N7147 N7034 N7023; Q9999 Q7476 Q7330

L101 ANSWER 2 OF 3 WPIDS COPYRIGHT 2003 THOMSON DERWENT on STN
AN 1993-160150 [20] WPIDS
DNN N1993-122892
TI Flashback-protected radiant gas burner tube - has internal sleeve supported by end **discs**, **carrying** granular charge inside perforated heat resistant tube.
DC Q73
IN SCHILLING, S W
PA (LUED-I) LUEDI R
CYC 11
PI DE 4136918 A1 19930513 (199320)* 5p F23D014-12
EP 542074 A2 19930519 (199320) DE 5p F23D014-16
R: AT BE CH DE DK FR GB IT LI NL SE
EP 542074 A3 19930804 (199507) F23D014-12
ADT DE 4136918 A1 DE 1991-4136918 19911111; EP 542074 A2 EP 1992-118706 19921102; EP 542074 A3 EP 1992-118706 19921102
PRAI DE 1991-4136918 19911111
REP No-SR.Pub; DE 2036510; DE 333171; FR 648608; US 3421826; US 4850862; US 5147201; WO 8606155
IC ICM F23D014-12; F23D014-16
ICS F23D014-46; F23D014-82
AB DE 4136918 A UPAB: 19931113
Two discs (18, 22) are retained inside the two ends of the perforated tube (10) for a radiant gas burner. They are secured by a tie rod (28) through the centre. The discs support a wire mesh sleeve (14) which forms a central space (20) and which carries a granular charge (16) inside the perforated tube, through which the fuel and air mixture can pass.

The perforated tube may be of sintered metal, ceramic material with holes made by a laser or a perforated steel tube or multiple layers of steel mesh. The granular charge may be of solid or hollow aluminium oxide spheres or sharp **edged** or **smooth** granules of e.g. glass or **quartz**.

USE/ADVANTAGE - Radiant gas burner tube in which flashback is prevented.

Dwg.1/1

ABEQ EP 542074 A UPAB: 19931113

Two discs (18, 22) are retained inside the two ends of the perforated tube (10) for a radiant gas burner. They are secured by a tie rod (28) through the centre. The discs support a wire mesh sleeve (14) which forms a central space (20) and which carries a granular charge (16) inside the perforated tube, through which the fuel and air mixture can pass.

The perforated tube may be of sintered metal, ceramic material with holes made by a laser or a perforated steel tube or multiple layers of steel mesh. The granular charge may be of solid or hollow aluminium oxide spheres or sharp **edged** or **smooth** granules of e.g. glass or **quartz**.

USE/ADVANTAGE - Radiant gas burner tube in which flashback is prevented.

Dwg.1/1

FS GMPI

FA AB; GI

L101 ANSWER 3 OF 3 WPIDS COPYRIGHT 2003 THOMSON DERWENT on STN

AN 1978-10015A [05] WPIDS

TI Semiconductor **wafer holder** - with three **quartz** arms extending from rod to engage minimal area of wafer periphery.

DC L03 U11

IN ANTHONY, T R; CLINE, H E

PA (GENE) GENERAL ELECTRIC CO ?

CYC 1

PI US 4068814 A 19780117 (197805)*

PRAI US 1976-733237 19761018

IC B01J017-12

AB US 4068814 A UPAB: 19930901

A semiconductor body holder, e.g. for zone melting, comprises a **quartz** rod with one end to support the holder and the other carrying three flexible **quartz** arms forming an **obtuse angle** with the base and each having at its distal end a refractory finger extending towards the rpd.

The orientation of the fingers, arms and rods minimises an shadowing effect of the arms on radiation emitted by a supported wafer and minimises inducement of undesirable thermal gradients in the wafer. Each finger engages only a minimal outer peripheral area of a wafer and each arm a minimal part of a wafer edge.

FS CPI EPI

FA AB

MC CPI: L03-D02B

=> file hca

FILE 'HCA' ENTERED AT 12:13:23 ON 25 JUL 2003

=> d l86 1-21 cbib abs hitstr hitind

L86 ANSWER 1 OF 21 HCA

137:354771 A method and apparatus for heating a gas-solvent solution. Boyers, David G. (Phifer Smith Corporation, USA). PCT Int. Appl. WO 2002089532 A1 20021107, 81 pp. DESIGNATED STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2002-US13261 20020426. PRIORITY: US 2001-PV287157 20010426.

AB A heating method quickly heats a gas-solvent soln., such as ozone-solvent soln., from a relatively low temp. T1 to a relatively high temp. T2, such that the gas-solvent soln. has a much higher dissolved gas concn. at temp. T2 than could be achieved if the gas-solvent soln. had originally been formed at the temp. T2. The method can be used for removing photoresist, post-ash photoresist residue, post-etch residue, and other org. materials from semiconductor **wafers**, flat panel display substrates, and the like, at high speed using a soln. of gas dissolved in a solvent, such as ozone dissolved in water. Various apparatuses, such as, a resistance heater, an induction heater, a microwave resonator and thermal contact heating by a heated fluid, etc., are also provided for **carrying** out the heating method. Each app. includes a heating vol. having an inlet for receiving a flowing gas-solvent soln. and an outlet for delivering the flowing gas-solvent soln.

IT **24937-79-9**, Pvdf
(PVDF, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)

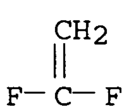
RN 24937-79-9 HCA

CN Ethene, 1,1-difluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 75-38-7

CMF C2 H2 F2

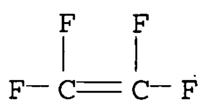


IT **9002-84-0**, Teflon
(TFE and PTFE, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)

RN 9002-84-0 HCA
CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



IC ICM H05B006-78
ICS H05B006-80; H05B006-10; C03C023-00
CC 47-4 (Apparatus and Plant Equipment)
Section cross-reference(s): 38, 56, 57
IT **Fluoropolymers**, uses
(PVDF, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)
IT **Fluoropolymers**, uses
(TFE and PTFE, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)
IT **24937-79-9**, Pvdf
(PVDF, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)
IT **9002-84-0**, Teflon
(TFE and PTFE, nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)
IT 14808-60-7, **Quartz**, uses
(nonmetallic heater components; method and app. for heating a gas-solvent soln. for cleaning electronic components)

L86 ANSWER 2 OF 21 HCA COPYRIGHT 2003 ACS on STN
137:193234 Recharge pipe for solid multi-crystal material, and single crystal producing method using the same. Iwasaki, Atsushi; Takeyasu, Shinobu (Shin-Etsu Handotai Co., Ltd., Japan). PCT Int. Appl. WO 2002068732 A1 20020906, 27 pp. DESIGNATED STATES: W: CN, JP, KR, US; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR. (Japanese). CODEN: PIXXD2. APPLICATION: WO 2002-JP1796 20020227. PRIORITY: JP 2001-55668 20010228.
AB An inexpensive recharge pipe for solid multi-crystal material that is capable of improving productivity of single crystal and a single crystal producing method using the same are described. The recharge pipe, which is removably installed in the single crystal producing device having a crucible contg. a crystal molten liq., is internally provided with a substantially cylindrical recharge pipe main body for **holding** a solid multi-crystal material therein: the recharge pipe main body gradually widening toward the lower end. The recharge pipe is further equipped with a conical valve removably disposed at the lower end of the recharge pipe main body, a lid removably disposed at the upper end of the recharge pipe main body,

a hook, a recharge pipe wire connecting the hook and the conical valve, and a stop for positioning the recharge pipe wire such that is extends through substantially the center of the recharge pipe main body.

IT **9002-84-0**, PTFE
(recharge pipe for solid multi-crystal material, and single crystal producing method using same)

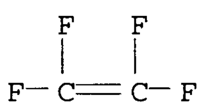
RN 9002-84-0 HCA

CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3

CMF C2 F4



IT **7440-21-3, Silicon, processes**
(recharge pipe for solid multi-crystal material, and single crystal producing method using same)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C30B015-00
ICS C30B029-06

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 47

IT **Fluoropolymers**, uses
(recharge pipe for solid multi-crystal material, and single crystal producing method using same)

IT 7631-86-9, Silica, uses
(**quartz**-type; recharge pipe for solid multi-crystal material, and single crystal producing method using same)

IT **9002-84-0**, PTFE
(recharge pipe for solid multi-crystal material, and single crystal producing method using same)

IT **7440-21-3, Silicon, processes**
(recharge pipe for solid multi-crystal material, and single crystal producing method using same)

L86 ANSWER 3 OF 21 HCA COPYRIGHT 2003 ACS on STN

137:162365 Semiconductor sputter-**etching** apparatus in prevention of contamination. Nakano, Yuichi (Sony Corp., Japan). Jpn. Kokai Tokkyo Koho JP 2002231692 A2 20020816, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2001-21860 20010130.

AB The title app. as a chamber has a top lid to cover the chamber-top

opening for vacuum sealing, a cylindrical **quartz** wall inside the chamber wall, and a plasma-**jig** attaching plate lined on the inside wall of the top lid. The lined top-lid inside wall is provided so that the distance between the inside surface of the cover and the top end of the lined plate is greater than that between the inside surface of the cover and the inside surface of the lined plate, sa as to effective shielding of product silica particles. The app. is used in removal of spontaneously formed oxide film on semiconductor substrates.

IC ICM H01L021-3065
CC 76-3 (Electric Phenomena)
ST spontaneous oxide removal sputter **etching** app contamination shield
IT Sputtering
 (**etching**; semiconductor sputter-**etching** app. in prevention of contamination)
IT Contamination (electronics)
 (prevention of, for environment and substrates; semiconductor sputter-**etching** app. in prevention of contamination)
IT **Etching**
 (sputter; semiconductor sputter-**etching** app. in prevention of contamination)
IT Semiconductor materials
 (substrates; semiconductor sputter-**etching** app. in prevention of contamination)
IT Sealing
 (vacuum, lids for; semiconductor sputter-**etching** app. in prevention of contamination)
IT 14808-60-7, **Quartz**, uses
 (lining wall; semiconductor sputter-**etching** app. in prevention of contamination)
IT 7440-21-3, **Silicon**, processes
 (semiconductor **wafers**, removal of oxide film on; semiconductor sputter-**etching** app. in prevention of contamination)
IT 7631-86-9, Silica, processes
 (spontaneously formed film; semiconductor sputter-**etching** app. in prevention of contamination)

L86 ANSWER 4 OF 21 HCA COPYRIGHT 2003 ACS on STN
137:9680 Manufacture of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon wafers**. Inaki, Kyoichi; Araki, Ifsuo (Heraeus Quarzglas Gmbh & Co. Kg, Germany; Shin-Etsu Quartz Products Co., Ltd.). Eur. Pat. Appl. EP 1213269 A1 20020612, 6 pp. DESIGNATED STATES: R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR. (English). CODEN: EPXXDW. APPLICATION: EP 2001-128581 20011130. PRIORITY: JP 2000-369534 20001205.

priority

AB The **fluororesin**-coated **quartz** glass **jig** is free from the coating peeling off by attacking hydrofluoric acid or from generating particles due to the **etching** of

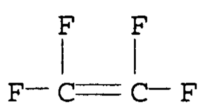
quartz glass, while yet preventing the generation of chipping by relaxing the impact imposed on the **quartz** glass by **silicon wafers**. The surface of the **quartz** glass **jig** is wholly covered with a pinhole-free **fluororesin** coating .gtoreq.50 .mu.m thick. The **fluororesin** is selected from tetrafluoroethylene resin, tetrafluoroethyleneperfluoroalkyl vinyl ether resin, perfluoroethylenepropylene resin, ethylenetetrafluoroethylene resin, chlorotrifluoroethylene resin, ethylenechlorotrifluoroethylene resin, vinylidene difluoride resin, vinyl fluoride resin, and tetrafluoroethyleneperfluorodioxol resin.

IT **25038-71-5**, Ethylenetetrafluoroethylene copolymer
25101-45-5, Ethylenechlorotrifluoroethylene copolymer
27029-05-6, Perfluoroethylenepropylene copolymer
(glass coating with; manuf. of acid-resistant **fluororesin** -coated **quartz** glass **jig** for use in cleaning **silicon wafers**)

RN 25038-71-5 HCA
CN Ethene, tetrafluoro-, polymer with ethene (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



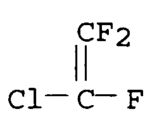
CM 2

CRN 74-85-1
CMF C2 H4

RN 25101-45-5 HCA
CN Ethene, chlorotrifluoro-, polymer with ethene (9CI) (CA INDEX NAME)

CM 1

CRN 79-38-9
CMF C2 Cl F3



CM 2

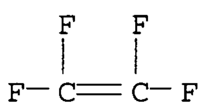
CRN 74-85-1
CMF C2 H4

$H_2C{=}CH_2$

RN 27029-05-6 HCA
CN 1-Propene, polymer with tetrafluoroethene (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



CM 2

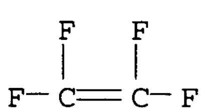
CRN 115-07-1
CMF C3 H6

$H_3C{-}CH{=}CH_2$

IT **9002-84-0**, Tetrafluoroethylene resin
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon wafers**)
RN 9002-84-0 HCA
CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



IT **7440-21-3, Silicon, processes**
(**silicon wafers**; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig**

for use in cleaning **silicon wafers**)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C03C017-32
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** glass **silicon wafer** cleaning
fluororesin coating; semiconductor device fabrication
silicon wafer cleaning
IT Coating materials
(acid-resistant; manuf. of acid-resistant **fluororesin**
-coated **quartz** glass **jig** for use in cleaning
silicon wafers)
IT **Semiconductor device fabrication**
(cleaning **silicon wafers**; manuf. of
acid-resistant **fluororesin**-coated **quartz**
glass **jig** for use in cleaning **silicon**
wafers)
IT **Fluoropolymers**, uses
(**fluororesin** coating; manuf. of acid-resistant
fluororesin-coated **quartz** glass **jig**
for use in cleaning **silicon wafers**)
IT **Etching**
(of **quartz** glass; manuf. of acid-resistant
fluororesin-coated **quartz** glass **jig**
for use in cleaning **silicon wafers**)
IT **Fluoropolymers**, uses
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf.
of acid-resistant **fluororesin**-coated **quartz**
glass **jig** for use in cleaning **silicon**
wafers)
IT 7631-86-9, Silicon dioxide, uses
(cryst. powder; manuf. of acid-resistant **fluororesin**
-coated **quartz** glass **jig** for use in cleaning
silicon wafers)
IT 75-02-5D, Vinyl fluoride, resin 75-38-7D, Vinylidene difluoride,
resin 79-38-9D, Chlorotrifluoroethylene, resin **25038-71-5**
, Ethylenetetrafluoroethylene copolymer **25101-45-5**,
Ethylenechlorotrifluoroethylene copolymer **27029-05-6**,
Perfluoroethylenepropylene copolymer
(glass coating with; manuf. of acid-resistant **fluororesin**
-coated **quartz** glass **jig** for use in cleaning
silicon wafers)
IT 52622-80-7, Dioxol
(**perfluoro-**, tetrafluoroethylene **resin**
contg., glass coating with; manuf. of acid-resistant
fluororesin-coated **quartz** glass **jig**
for use in cleaning **silicon wafers**)

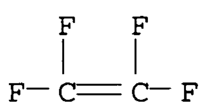
IT **9002-84-0**, Tetrafluoroethylene resin
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon** **wafers**)
IT 7664-39-3, Hydrofluoric acid, **processes**
(pickling of **silicon wafers** by; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon** **wafers**)
IT 60676-86-0, Silica, vitreous
(**quartz** glass **jig**; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon wafers**)
IT **7440-21-3, Silicon, processes**
(**silicon wafers**; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon wafers**)
IT 12125-01-8, Ammonium fluoride
(soln. contg. HF and ammonium fluoride; manuf. of acid-resistant **fluororesin**-coated **quartz** glass **jig** for use in cleaning **silicon wafers**)

L86 ANSWER 5 OF 21 HCA COPYRIGHT 2003 ACS on STN
136:220626 **Quartz** glass tool having high plasma resistance for plasma-processing apparatus. Inagi, Yasukazu (Shin-Etsu Quartz Products Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2002068766 A2 20020308, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2000-259645 20000829.
AB The tool has surface roughness Ra 5-0.05 .mu.m, no. of surface micro crack .ltoreq.500 /cm2, and H2O concn. .gtoreq.5 .times. 1016 mol./cm3. The tool is useful for **etching** a silicone **wafer**.
IC ICM C03B020-00
ICS C03B020-00; C03C015-00; H01L021-3065
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** glass tool plasma resistance; silicone **wafer** plasma **etching** app **quartz** glass; hydrogen contg **quartz** glass **jig**
IT **Etching** apparatus
(plasma, for silicone **wafer**; **quartz** glass tool having high plasma resistance for plasma-processing app.)
IT **Jigs**
(**quartz** glass tool having high plasma resistance for plasma-processing app.)
IT 1333-74-0, Hydrogen, uses
(**quartz** glass tool having high plasma resistance for plasma-processing app.)
IT 60676-86-0P, **Quartz** glass
(**quartz** glass tool having high plasma resistance for plasma-processing app.)

L86 ANSWER 6 OF 21 HCA COPYRIGHT 2003 ACS on STN
136:104337 Process equipment for fabricating semiconductor device. Kim, Gwang Sik (Samsung Electronics Co., Ltd., S. Korea). Repub. Korean Kongkae Taeho Kongbo KR 2000020886 A 20000415, No pp. given (Korean). CODEN: KRXXA7. APPLICATION: KR 1998-39677 19980924.
AB A process equipment for fabricating a semiconductor device is provided to prevent a pressure state of a **quartz** chamber from changing caused by attack resulting from repeated contact of a teflon ring with a **chuck** thereunder. A processing equipment for fabricating a semiconductor device comprises a **quartz** chamber, a teflon ring, a **chuck**, and a supporter. A semiconductor fabricating process is performed in the **quartz** chamber. The **chuck** inserts and ejaculates a **wafer** in the **quartz** chamber by performing up-and-down movement under the teflon ring closely adhered to a lower portion of the **quartz** chamber. The supporter contacts with the **chuck** under the teflon ring.
IT **9002-84-0**, Teflon
(ring; process equipment for fabricating semiconductor device)
RN 9002-84-0 HCA
CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



IC ICM H01L021-20
CC 47-10 (Apparatus and Plant Equipment)
Section cross-reference(s): 76
ST app semiconductor device fabrication **quartz** chamber teflon ring **chuck**
IT Apparatus
Semiconductor device fabrication
(process equipment for fabricating semiconductor device)
IT **Fluoropolymers**, uses
(ring; process equipment for fabricating semiconductor device)
IT 14808-60-7, **Quartz**, uses
(chamber; process equipment for fabricating semiconductor device)
IT **9002-84-0**, Teflon
(ring; process equipment for fabricating semiconductor device)

L86 ANSWER 7 OF 21 HCA COPYRIGHT 2003 ACS on STN
135:297109 Reaction chamber with at least one high-frequency(HF) lead.. Franken, Walter; Strauch, Gerd; Kaeppeler, Johannes; Juergensen, Holger (Aixtron A.-G., Germany). PCT Int. Appl. WO 2001078105 A1

20011018, 22 pp. DESIGNATED STATES: W: JP, KR, US; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR. (German). CODEN: PIXXD2. APPLICATION: WO 2001-DE1450 20010412. PRIORITY: DE 2000-10018127 20000412.

AB The invention relates to a reaction chamber esp. for **carrying** out substrate coating methods, such as CVD methods, characterized in that .gtoreq.1 opening is provided in .gtoreq.1 outer wall in which an HF and esp. a radio-frequency(RF) lead is inserted in a pressure or vacuum tight manner. The inventive reaction chamber is further characterized by a combination of the following features: a support plate is inserted and sealed in every opening; the support plate has .gtoreq.1 opening for an HF line; every HF line is provided with a collar in the zone disposed in the reaction chamber, a 1st seal being mounted on the collar; a 1st **disk** from an insulating material is inserted between a 2nd seal on the support pate and the 1st seal on the collar; a thread is provided in the zone outside the reaction chamber of every HF line, a screw element being screwed onto the thread in such a manner that it seals and forces the collar of the HF line against the insulating **disk** via the 1st seal and the **disk** against the support plate via the 2nd seal, without an elec. contact between the HF line and the support plate being established or an arc-over occurring between the HF line and the support plate.

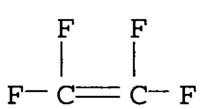
IT **9002-84-0**, Teflon
(case; reaction chamber with at least one high-frequency(HF) feedthrough)

RN 9002-84-0 HCA

CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



IC ICM H01J037-32

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 42

IT **Fluoropolymers**, processes
(case; reaction chamber with at least one high-frequency(HF) feedthrough)

IT **Disks**
(**quartz**; reaction chamber with at least one high-frequency(HF) feedthrough)

IT **9002-84-0**, Teflon
(case; reaction chamber with at least one high-frequency(HF) feedthrough)

IT 14808-60-7, **Quartz**, processes

(**disk** as insulator; reaction chamber with at least one high-frequency(HF) feedthrough)

L86 ANSWER 8 OF 21 HCA COPYRIGHT 2003 ACS on STN
135:276722 Manufacture of rounded **quartz** tubes. Matsutani, Toshikatsu; Takahashi, Shoji; Ise, Yoshiaki (Shin-Etsu Quartz Products Co,. Ltd. Yamagata, Japan; Shin-Etsu Quartz Products Co., Ltd.). Jpn. Kokai Tokkyo Koho JP 2001270727 A2 20011002, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2000-89412 20000328.
AB The manuf. of rounded **quartz** tubes involves depositing a **corner-rounded quartz** thick **disk** on a **quartz** cylinder having a corresponding diam., wherein the process involves beveling the peripheral edge, polishing for leveling of the melt-depositing surface of the **disk** and the tube end, melt-depositing the **disk** on the tube end, and heating the deposited portion to be softened and covering the portion with a rounded **jig** to give rounded end. The process provides easy formation of smooth rounded **quartz** tubes useful for semiconductor manufg.
IC ICM C03B023-13
ICS B24B007-24; C03B020-00
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** tube round melt deposition **jig** semiconductor manufg
IT Polishing
(depositing ends; manuf. of rounded **quartz** tubes)
IT Heating
(for softening; manuf. of rounded **quartz** tubes)
IT Semiconductor materials
(manufg. app., **quartz** tubes for; manuf. of rounded **quartz** tubes)
IT Pipes and Tubes
(rounded end-sealed tubes, manuf. of; manuf. of rounded **quartz** tubes)
IT **Jigs**
(rounded; manuf. of rounded **quartz** tubes)
IT 14808-60-7, **Quartz**, properties
(manuf. of rounded **quartz** tubes)

L86 ANSWER 9 OF 21 HCA COPYRIGHT 2003 ACS on STN
134:151418 Preparation of silicon carbide ceramics by water dispersion-reaction sintering. Wu, Qide; Wei, Mingkun; Wang, Huaide; Han, Jianjun; Hong, Xiaoming (Wuhan University of Technology, Peop. Rep. China). Faming Zhuanli Shenqing Gongkai Shuomingshu CN 1264687 A 20000830, 7 pp. (Chinese). CODEN: CNXXEV. APPLICATION: CN 2000-114425 20000315.
AB The **process** comprises **firing** industrial C or graphite at 1000-1200.degree. for 1-4 h (isolated from O), crushing to 1-2 mm, adding water (dispersing agent), binder, plasticizer, and de-foaming agent, ball milling, dilg., classifying to obtain C slurry (d90 = 45 .mu.m; d10 = 5 .mu.m); forming to obtain blanks,

drying, loading into graphite crucible in induction furnace, covering with Si powder (the ratio of C : Si = 1 : 2.5), heating in vacuum at 150-200.degree./h to 1550-1650.degree., and **holding** for 1-2 h, where the blanks can also be treated by gas phase siliconizing at 1800-2050.degree. in Ar. Preferably, the content, particle size, and particle size distribution of C structure, and the pore size of the blanks are controlled by adjusting the particle size and amt. of C powder, ablative material, and filler; the ablative material is wood powder, walnut shell powder, plastic powder, **quartz** powder, or white C black; and the filler is Si powder with d90 = 7 .mu.m. The obtained ceramics have low prodn. cost.

IT **7440-21-3, Silicon, processes**
(starting material; for prepn. of silicon carbide ceramics by water dispersion-reaction sintering)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C04B035-573

CC 57-2 (Ceramics)
Section cross-reference(s): 38

IT 14808-60-7, **Quartz**, uses
(ablative material; for prepn. of silicon carbide ceramics by water dispersion-reaction sintering)

IT **7440-21-3, Silicon, processes**
7440-44-0, Carbon, processes 7782-42-5, Graphite, processes
(starting material; for prepn. of silicon carbide ceramics by water dispersion-reaction sintering)

L86 ANSWER 10 OF 21 HCA COPYRIGHT 2003 ACS on STN

133:244268 Building passive components with silica waveguides. Sun, Jacob C. K.; Schmidt, Kevin M. (Photonic Integration Research, Inc. (PIRI), Columbus, OH, USA). Proceedings of SPIE-The International Society for Optical Engineering, 3795(Terahertz and Gigahertz Photonics), 313-319 (English) 1999. CODEN: PSISDG. ISSN: 0277-786X. Publisher: SPIE-The International Society for Optical Engineering.

AB A review with 6 refs. Low cost and reliable passive components are essential to further span the use of fiber optics and realize the all- optical communication networks. SiO2 waveguide technol. has played an important role in the development of passive components. Devices of 1 X N, 2 X N splitters, and 1.3/1.55 WDMs were mass-produced for practical applications. Recently, large vols. of array waveguide gratings also were produced for dense WDM applications. The optical fiber preform manufg. **process**, **flame** hydrolysis deposition is adapted to deposit low loss SiO2 glass on planar **substrates** (**Si**, **quartz** or alumina ceramics). Photolithog. and reactive ion **etching** is then applied to pattern various types of

integrated waveguide circuits. Testing, fiber-connecting, and device packaging follow the circuit fabrication to produce the fiber- pigtailed modules. The technol. provides a versatile means of building passive components. The manufg. processes are reviewed and the functions and performance of various circuits are discussed with an emphasis on the current status of the array waveguide gratings.

CC 73-0 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

IT Sputtering
Sputtering
(**etching**, reactive; building passive components with silica waveguides)

IT **Etching**
Etching
(sputter, reactive; building passive components with silica waveguides)

L86 ANSWER 11 OF 21 HCA COPYRIGHT 2003 ACS on STN

ref

132:111873 Manufacture of **quartz** glass **jigs** for semiconductor **wafer** treatment. Matsuda, Satoshi; Kondo, Kazuyoshi; Abe, Emiko (Nippon Sekiei Glass K. K., Japan). Jpn. Kokai Tokkyo Koho JP 2000016821 A2 20000118, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-188409 19980703.

AB The **jigs** are manufd. by: grinding a **quartz** glass part to form a groove, removing the surface grease, and surface finishing. Preferably, the grease is removed by using a surfactant or by firing. Contamination is prevented during treating the semiconductor **wafers**.

IC ICM C03B020-00
ICS B08B003-08; B08B003-10; H01L021-304; H01L021-68

CC 57-1 (Ceramics)
Section cross-reference(s): 76

ST **quartz** glass **jig** semiconductor **wafer** treatment contamination prevention; grease removal **jig** manuf

IT **Jigs**
Semiconductor materials
(manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination prevention)

IT Contamination (electronics)
(removal of; manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination prevention)

IT 7664-39-3, Hydrofluoric acid, processes
(**etching** soln. contg.; in manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination prevention)

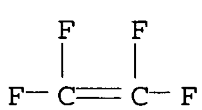
IT 60676-86-0, **Quartz** glass
(manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination

prevention)
IT 255373-08-1, Deberu
(surfactant, for removal of grease; in manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination prevention)
IT 7782-40-3, Diamond, uses
(wheels; for forming of groves on **jigs** in manuf. of **quartz** glass **jigs** for semiconductor **wafer** treatment for contamination prevention)

L86 ANSWER 12 OF 21 HCA COPYRIGHT 2003 ACS on STN
131:26635 Plasma reactor with a deposition shield for processing semiconductor **wafers**. DeOrnellas, Stephen P.; Ditizio, Robert A. (Tegal Corporation, USA). PCT Int. Appl. WO 9929923 A1 19990617, 38 pp. DESIGNATED STATES: W: CA, CN, JP, KR; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2. APPLICATION: WO 1998-US25437 19981201. PRIORITY: US 1997-985730 19971205.
AB A reactor includes a shield which prevents the deposition, e.g., by sputtering, of materials along a line-of-sight path from a **wafer** toward and onto an electrode or a window which couples the electrode to a reaction chamber of the reactor.
IT **9002-84-0**
(plasma reactor with a deposition shield contg.)
RN 9002-84-0 HCA
CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3
CMF C2 F4



IC ICM C23C016-00
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST plasma reactor deposition shield; semiconductor **wafer** processing plasma reactor
IT **Holders**
(**chucks**; plasma reactor with a deposition shield contg.)
IT **Fluoropolymers**, uses
Organic compounds, uses
Polyamides, uses
Polyimides, uses
Polyoxymethylenes, uses
(plasma reactor with a deposition shield contg.)
IT Semiconductor materials

Shields
(plasma reactor with a deposition shield for processing semiconductor **wafers**)
IT Reactors
(plasma; plasma reactor with a deposition shield for processing semiconductor **wafers**)
IT 7429-90-5, Aluminum, uses 7440-21-3, Silicon, uses 7440-44-0, Carbon, uses **9002-84-0**
(plasma reactor with a deposition shield contg.)
IT 7631-86-9, Silica, uses
(**quartz**; plasma reactor with a deposition shield contg.)

L86 ANSWER 13 OF 21 HCA COPYRIGHT 2003 ACS on STN
130:244862 In-situ shallow trench isolation **etch** with clean chemistry. Wang, Xikun; Williams, Scott; Padmapani, Nallan; Pan, Shaoher (Silicon Etch Division, Applied Materials, Inc., Sunnyvale, CA, 95054, USA). IEEE/CPMT International Electronics Manufacturing Technology Symposium, 23rd, Austin, Tex., Oct. 19-21, 1998, 150-154. Institute of Electrical and Electronics Engineers: New York, N. Y. (English) 1998. CODEN: 67HHAB.
AB An in-situ hard-mask open and self-clean shallow trench isolation (STI) **etch** process with a bromine and fluorine based chem. was developed using an Applied Materials DPS chamber. SEM micrographs from an **etched** photoresist-patterned **wafer** show a desired trench profile with **rounded** bottom **corners** and **smooth** side walls. **Quartz** crystal micro-balance (QCM) measurements, coupon tests, and a 1000 **wafer** extended run demonstrate a clean STI process. No dry clean are necessary. The STI step used a chem. which balanced oxygen passivation with fluorine based **etching**. More tapered profiles can be achieved by increasing the O2 flow rate. Also, the side wall passivation and oxidn. improve the bottom **corner rounding**, which is desired to minimize stress and current leakage. Fluorine radicals chem. **etch** the silicon. With increasing fluorine content, the formation of side wall passivation becomes less pronounced, and therefore the profile becomes more vertical. This strategy balancing chem. **etchants**, passivators, energetic ions enables tuning of the profile within wide range. In addn. to chem., the source power and bias power were all varied. The of these parameters on the trench profile **angles** **corner rounding** and microloading are discussed. The simplicity, cleanliness, and excellent profile performance of the process make it a most promising candidate for sub-micron STI manufg.
CC 76-3 (Electric Phenomena)
ST hard mask shallow trench isolation **etching**
IT **Etching**
Leakage current
Passivation
Scanning electron microscopy

Semiconductor device fabrication
(In-situ shallow trench isolation **etch** with clean chem.)

IT Photoresists
(mask; In-situ shallow trench isolation **etch** with clean chem.)

L86 ANSWER 14 OF 21 HCA COPYRIGHT 2003 ACS on STN

130:244861 In-situ nitride mask open. Williams, Scott (Silicon Etch Division, Applied Materials, Inc., Sunnyvale, CA, 94086, USA). IEEE/CPMT International Electronics Manufacturing Technology Symposium, 23rd, Austin, Tex., Oct. 19-21, 1998, 146-149. Institute of Electrical and Electronics Engineers: New York, N. Y. (English) 1998. CODEN: 67HHAB.

AB As feature size approaches 0.25.box.m and below, shallow trench isolation (STI) has become the most favorable isolation scheme. One challenge in the development of a prodn.-worthy STI process is to combine the hard mask open and STI step into a single **etch** chamber. An STI process with an in situ hard mask open will provide lower cost of ownership as well as higher throughput. Chamber cleanliness is another crit. issue for STI processes using conventional **etchants** of HBr, Cl2, and O2. HBr related **etch** byproducts usually result in severe deposition inside the chamber, thus causing particle problems. This paper describes a nitride mask open process using a clean fluorine-based chem. which was successfully integrated into an STI process. However, the aggressive nature of the fluorine-based chem. also attacks the photoresist and tends to **etch** the nitride isotropically. Therefore, it is essential to choose process parameters that maximize the selectivity to photoresist and yield the most vertical nitride **etch**. Source power, bias power, gas flow, and pressure were all studied to maximize process performance. A typical sample consisted of an 8" **silicon wafer** with 25 nm of thermally grown oxide, 200 nm of nitride, and a 700. nm DUV photoresist mask. SEM micrographs were used to monitor the effects on profile **angle**, **corner rounding**, selectivity, and microloading. **Quartz** crystal monitor data and a 1000 **wafer** burn in both indicate that there is no deposition on the dome chamber walls.

CC 76-3 (Electric Phenomena)

IT Controlled atmospheres
Etching
Resists
Semiconductor device fabrication
(shallow trench isolation process with in-situ nitride mask)

L86 ANSWER 15 OF 21 HCA COPYRIGHT 2003 ACS on STN

128:298429 Manufacture of high-purity **quartz jigs** used for heat treatment of **silicon wafer**. Yoshikawa, Jun; Takeda, Takaji; Ariga, Shoji; Ikuno, Hiroto (Toshiba Ceramics Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 10114532 A2 19980506 Heisei, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP

1996-281594 19961004.

AB The method of manufg. the title **jigs** for treating **Si wafers** at .gtoreq.1100.degree. involves the step of **etching** the surface of a molded **quartz jig** with hydrofluoric acid to remove metal impurities. The **jigs** are useful as reactor core tubes, **wafer** boats, lagging materials, etc. giving no contamination to **Si wafers** under H annealing.

IC ICM C03B020-00
ICS C03C015-00; H01L021-205; H01L021-22; H01L021-31; H01L021-324

CC 57-1 (Ceramics)
Section cross-reference(s): 76

ST **etching** impurity removal **quartz jig** semiconductor; vitreous silica **silicon wafer** heat treatment

IT Pipes and Tubes
(heat treatment furnace; metal impurities removal by **etching** in manuf. of **quartz jigs** used for heat treatment of **Si wafer**)

IT **Etching**
Jigs
Semiconductor device fabrication
(metal impurities removal by **etching** in manuf. of **quartz jigs** used for heat treatment of **Si wafer**)

IT 7664-39-3, Hydrofluoric acid, processes
(**etching** liq. contg.; metal impurities removal by **etching** in manuf. of **quartz jigs** used for heat treatment of **Si wafer**)

IT 60676-86-0, Silica, vitreous
(metal impurities removal by **etching** in manuf. of **quartz jigs** used for heat treatment of **Si wafer**)

L86 ANSWER 16 OF 21 HCA COPYRIGHT 2003 ACS on STN

123:120917 Method and apparatus for manufacture of **quartz** glass substrates. Higuchi, Keiichi; Kikuchi, Fujio; Okano, Hiroaki (Hitachi Cable, Japan). Jpn. Kokai Tokkyo Koho JP 07157334 A2 19950620 Heisei, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1993-307802 19931208.

AB The title glass substrates are manufd. by: depositing glass fine particles on a substrate to form a deposition layer, and vitrifying by heating in an elec. furnace, where the heating is conducted by placing the substrate on an oxide-coated support. The support is made of SiC.

IC ICM C03C017-04
ICS C03B008-04; C03B037-018; H05K001-03

CC 57-1 (Ceramics)

ST **quartz** glass substrate manuf heating; silicon carbide support heating

IT **Firing**, heat-**treating process**
(oxide-coated **silicon** carbide support in method and

app. for manuf. of **quartz** glass substrates)
IT **Holders**
(**jigs**, oxide-coated silicon carbide support in method and app. for manuf. of **quartz** glass substrates)
IT 409-21-2, Silicon carbide, properties
(oxide-coated silicon carbide support in method and app. for manuf. of **quartz** glass substrates)
IT 60676-86-0, **Quartz** glass
(oxide-coated silicon carbide support in method and app. for manuf. of **quartz** glass substrates)

L86 ANSWER 17 OF 21 HCA COPYRIGHT 2003 ACS on STN
119:239468 Heat treatment of semiconductor **wafers**. Habu, Yoshio (Kansai Nippon Electric, Japan). Jpn. Kokai Tokkyo Koho JP 05062921 A2 19930312 Heisei, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1991-220236 19910830.
AB A **boat**, preferably from **quartz**, coated with a polysilicon film, is used. The loss of a semiconductor **wafer** with the **boat** in heat treatment is prevented.
IC ICM H01L021-22
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57
ST heat treatment semiconductor **wafer**; **quartz** polysilicon coating **boat**
IT **Firing**, heat-**treating process**
(of semiconductor **wafers**, polysilicon-coated **quartz boat** for)
IT Coating materials
(polysilicon, on **quartz boat** for heat treatment of semiconductor materials)
IT Semiconductor materials
(**wafers**, polysilicon-coated **quartz boat** for heat treatment for)
IT 7440-21-3, Silicon, uses
(poly-, coating on **quartz boat** for heat treatment of semiconductor **wafers**)
IT 14808-60-7, **Quartz**, uses
(polysilicon-coated **boat** from, for heat treatment of semiconductor **wafers**)

L86 ANSWER 18 OF 21 HCA COPYRIGHT 2003 ACS on STN
111:160303 Dental alloy composites containing a noble metal-containing core coated with a heat-protective metal layer prior to silanization via **flame** hydrolysis **process**. Schmidt, Albert; Tiller, Hans Juergen; Goebel, Roland; Wowra, Hans Juergen; Hilpmann, Bernd; Magnus, Brigitte (Kulzer und Co. G.m.b.H., Fed. Rep. Ger.). Eur. Pat. Appl. EP 298190 A1 19890111, 9 pp. DESIGNATED STATES: R: AT, CH, DE, FR, IT, LI. (German). CODEN: EPXXDW. APPLICATION: EP 1988-102661 19880224. PRIORITY: DD 1987-303602 19870609.
AB A dental composite, esp. for dental replacements, comprises a noble metal-contg. **carrier** layer which contains at its

surface a silanized **Si** or Si oxide-contg. cover layer which itself carries a plastic layer. The **carrier** comprises .gtoreq.20% by wt. Ag and .gtoreq.20% by wt. Pd and the sum of Ag and Pd is .gtoreq.50%. A heat-protective layer consisting of a metal selected from Sn, Cr, Cu, Ag, Ni, Zn, or Au is positioned between the cover layer and the noble metal-contg. **carrier** layer. A dental **carrier** compn. consisting of an alloy contg. 70% by wt. Ag and 30% by wt. Pd was placed into an electrolysis bath contg. CrO3 8.0, K2Cr2O7 2.0, and Cr2(SO4)3 0.1 g/L; the c.d. was 10 mA/cm2, voltage 10 V, and galvanization time 5 min. The coated **carrier** was coated with a Si oxide (SiOx-C-layer) layer using a flame hydrolysis torch, silanized, and coated with an opacifying layer (i.e. Dentacolor) and coated with a 3 mm thick plastic layer. In the electrolytically Cr-plated compn. no crack-formation was evident. The shear strength of the SiOx-C-coated Cr layer-contg. (50 .mu.m thickness) composite was 1660 N/cm2 after boiling said compn.; the shear strength of a Ni-coated **carrier** was 1530 N/cm2. The shear strength of a **carrier** without the heat-protective coating was 850 N/cm2. Coating with SiOx is effected using a high-frequency magnetron sputtering device which deposits SiOx from highly purified **quartz** in a vacuum onto the dental prosthesis. Dental prosthesis comprising plastic coatings on the dental materials consisting of Ag/Pd alloys with a high content or Ag and Si- or Si oxide-contg. coating layer show an improved adhesive strength of their plastic coatings; however, their adhesive strength is not as high as is seen with dental materials consisting of **carriers** made from different metals. This is explained by a segregation of the Ag/Pd alloy when the Si- or Si oxide-contg. layer is applied using a flame hydrolysis torch and exposed to high temps. briefly. This is esp. the case for alloys contg. 40-75% by wt. Ag and 20-30% Pd.

IC ICM A61K006-04
ICS A61C013-08
CC 63-7 (Pharmaceuticals)

L86 ANSWER 19 OF 21 HCA COPYRIGHT 2003 ACS on STN
94:113409 Chemical **etch** polishing of semiconductors. D'Asaro, Lucian A. (Bell Telephone Laboratories, Inc., USA). U.S. US 4244775 19810113, 6 pp. (English). CODEN: USXXAM. APPLICATION: US 1979-34491 19790430.

AB Semiconductors such as GaAs are thinned and polished by using a chem. **etchant** (a H2O2-H2SO4-H2O soln.) in conjunction with a grooved flat polishing plate. The polishing plate has a hardness >2 on the mohs scale. **Quartz** can be used. Excellent polishing without objectionable **edge rounding** occurs. For example, a 15-mil-thick Cr-doped GaAs **wafer** approx. 0.5 in. in diam. was **etched**. by using a glass plate 8 in. in diam. and 0.25 in. thick having a width of 30 mils and 30-mils-deep grooves spaced approx. 0.25 in. center to center. The grooves were cut in a checkerboard pattern. The **etchant** used was a soln. of 3 parts of concd. H2SO4, 1 part of 30% H2O2, and

1 part of distd. deionized H2O.
IC H01L021-306
NCL 156636000
CC 76-13 (Electric Phenomena)
IT Polishing
(of semiconductors using polishing plate and chem. **etchant**)
IT Semiconductor materials
(polishing of, using polishing plate and chem. **etchant**)
IT 1303-00-0, uses and miscellaneous
(polishing of, using polishing plate and chem. **etchant**)

L86 ANSWER 20 OF 21 HCA COPYRIGHT 2003 ACS on STN
85:185412 Acoustic waveguide fabrication by orientation dependent **etching**. Wagers, Robert S.; Weirauch, Donald F. (Texas Instrum. Inc., Dallas, TX, USA). Ultrasonics Symposium Proceedings 539-43 (English) 1975. CODEN: ULSPDT. ISSN: 0090-5607.
AB Acoustic waveguides of LiNbO3 and **quartz** were examd. The guides studied have wedge-shaped cross sections with 1 surface coplanar with the top surface of the substrate **wafer**. The waveguides are formed by using orientation-dependent **etchants** to selectively **etch** the top surface of the **wafer**, leaving wedge-shaped overhanging structures for wave guiding. Waveguides with top angles of .apprx.60.degree. and lateral surface dimensions on the order of 25 .mu. were **etched** on **quartz**. The lateral surface **smoothness** and **apex** roughness of the guides are less than 0.1 micron. Similar guides were **etched** in LiNbO3 but the lateral surface smoothness results are currently limited by **etch** mask erosion. Low frequency prototype waveguides with wedge-shaped geometries were fabricated and tested. Results at 1 MHz on PZT show that extremely high impedances are encountered. If impedance matching is **carried** out and the transducers are fabricated with concern for spurious pad modes, then insertion losses under 10 dB (including the matching networks) are easily obtainable. In addn., the responses are free from spurious modes with rejection in excess of 50 dB at the zeros of the transducer spectrum.
CC 76-6 (Electric Phenomena)
IT Waveguides
(acoustic, **etching** of lithium niobate crystals for)
IT 12031-63-9
(acoustic waveguides, fabrication and **etching** of)

L86 ANSWER 21 OF 21 HCA COPYRIGHT 2003 ACS on STN
71:17796 Formation and quenching of ortho-positronium in molecular materials. Lagu, R. G.; Kulkarni, V. G.; Thosar, B. V.; Chandra, G. (Inst. Fudam. Res., Bombay, India). Proceedings - Indian Academy of Sciences, Section A, 69(1), 48-65 (English) 1969. CODEN: PISAA7. ISSN: 0370-0089.
AB The title study was **carried** out by placing a thin 22Na source, deposited on a poly(ethylene terephthalate) (Mylar) film,

between 2 **disks** (.apprx.2 mm. thick) of the mol. material. The 1280-kev. and 511-kev. .gamma.-radiation emitted by the 22Na on e+ emission and annihilation, resp., were used to detect these events. The delayed coincidence between the 2 .gamma.-rays was observed, and the time distribution of the delayed component was used to det. the effective lifetime (.tau.2) of the orthopositronium in the sample and the intensity (I2), which was the ratio of the 2-photon events owing to the quenching of the triplet positronium to the total no. of 2-photon events in the process. A .tau.2 component was found for mol. materials, including liq. and amorphous systems, semicryst. polymers, and mol. crystals (material, sec. .times. 109 .tau.2, and %I2 given): cyclooctatetraene, 3.1, 29; benzene, 2.7, 28; liq. naphthalene, 2.6, 3; iso-PrOH, 2.3, 30; polystyrene, 2.2, 34; fused **quartz**, 1.8, 36; poly(tetrafluoroethylene) (Teflon), 3.5, 17; poly(Me methacrylate) (Lucite), 2.5, 21; polyethylene, 2.2, 22; poly-(vinyl chloride), 1.9, 26; Sb4O6, 3.1, 5; poly(oxymethylene), 2.1, 9; stilbene, 1.8, 6; naphthalene, 1.2, 10; phenanthrene, 1.2, 14. A correlation was observed between .tau.2 and I2, and an empirical model utilizing free vol. was developed to explain the correlation. The variations in .tau.2 and I2 with temp., pressure, melting of crystals, and the glass transition in polymers were discussed on the basis of the model. The inhibition of positronium formation in the org. liqs. PhF, PhCl, PhBr, PhI, o-xylene, m-xylene, and p-xylene was observed. The order of inhibition was related to increasing dipole moment or structural asymmetry. The 3-photon annihilation intensity (I3) was cald. for the materials studied and generally increased with increasing .tau.2. The increase in I3 with increasing temp. is discussed in terms of the model.

IT **9002-84-0**, properties
   (orthopositronium lifetime in)

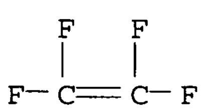
RN 9002-84-0 HCA

CN Ethene, tetrafluoro-, homopolymer (9CI) (CA INDEX NAME)

CM 1

CRN 116-14-3

CMF C2 F4



CC 75 (Nuclear Phenomena)

IT 588-59-0 629-20-9 1309-64-4, properties 9002-81-7 **9002-84-0**, properties 9002-86-2, properties 9002-88-4, properties 9003-53-6, properties 9011-14-7, properties 14808-60-7, properties
   (orthopositronium lifetime in)

=> d l87 1-30 cbib abs hitstr hitind

L87 ANSWER 1 OF 30 HCA COPYRIGHT 2003 ACS on STN

138:279889 Method and apparatus for removal of surface deposits from substrates for electronic devices. Kono, Shigeru (Nomura Micro Science Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2003103228 A2 20030408, 17 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2001-304078 20010928.

AB An O3-contg. gas and an org. acid-contg. washing soln., or the washing soln. contg. O3, is sprayed on a spinning substrate for cleaning it in a short time without residues. The app. equipped with a substrate holder, nozzles for the washing soln. and/or the O3-contg. gas, and a **jig** for fixing or moving the nozzles is also claimed.

IT **7440-21-3, Silicon, processes**
(**wafer** for semiconductor device; spraying of O3 gas and org. acid-contg. washing soln. to spinning substrates for electronic devices for removal of surface deposits)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM B08B003-08
ICS B08B003-02; C11D007-08; C11D007-18; C11D007-26; C11D017-08; G03F007-42; H01L021-027; H01L021-304

CC 76-14 (Electric Phenomena)

IT 7631-86-9, Silica, processes
(**quartz**-type, substrate for photomask; spraying of O3 gas and org. acid-contg. washing soln. to spinning substrates for electronic devices for removal of surface deposits)

IT **7440-21-3, Silicon, processes**
(**wafer** for semiconductor device; spraying of O3 gas and org. acid-contg. washing soln. to spinning substrates for electronic devices for removal of surface deposits)

L87 ANSWER 2 OF 30 HCA COPYRIGHT 2003 ACS on STN

138:220894 Application of XRF, XRD, thermal analysis, and voltammetric techniques to the study of ancient ceramics. Sanchez Ramos, S.; Bosch Reig, F.; Gimeno Adelantado, J. V.; Yusa Marco, D. J.; Domenech Carbo, A. (Faculty of Chemistry, Department of Analytical Chemistry, University of Valencia, Burjasot, 46100, Spain). Analytical and Bioanalytical Chemistry, 373(8), 893-900 (English) 2002. CODEN: ABCNBP. ISSN: 1618-2642. Publisher: Springer-Verlag.

AB An in-depth chem.-anal. study has been performed on biscuit and mortar from the 17th-18th century tiles from a medieval heritage in the province of Valencia, Spain. Representative samples were chosen from the tile fragments available, using appearance, essentially color and consistency, as the criterion. The chem. compn. was analyzed by x-ray fluorescence of the samples in the form of glass **disks** after a previous qual. study to choose the std.

materials for calibration and the exptl. conditions used in the anal. X-ray diffraction of the samples provided information about the mineralogical compn. which was consistent with the firing of the original materials. It also gave information about the range of temps. used in the firing. From thermal gravimetric anal. of the limestone, and from historical considerations, it was possible to deduce the raw materials used and their approx. compn. in the tiles. In the same way, it was possible to detd. the nature of the mortars used to fix the tiles. Cyclic voltammetric study of the iron (II) and iron (III) system in the biscuit showed the simultaneous presence of both oxidn. states, corroborating results.

CC 20-3 (History, Education, and Documentation)
Section cross-reference(s): 57

IT Archaeology
Ceramics
Firing (heat **treating**)
Thermogravimetric analysis
Voltammetry
X-ray diffraction
X-ray fluorescence
(study of ancient ceramics using XRF, XRD, thermal anal. and voltammetric techniques)

IT 1302-56-3, Gehlenite 1305-78-8, Calcium oxide, occurrence 1309-37-1, Iron oxide, occurrence 1309-48-4, Magnesium oxide (MgO), occurrence 1313-59-3, Sodium oxide (Na2O), occurrence 1314-56-3, Phosphorus oxide (P2O5), occurrence 1317-60-8, Hematite, occurrence 1318-74-7, Kaolinite, occurrence 1344-28-1, Aluminum oxide, occurrence 7439-89-6, Iron, occurrence 7446-11-9, Sulfur trioxide, occurrence 7631-86-9, Silica, occurrence 12136-45-7, Potassium oxide (K2O), occurrence 12172-80-4, Augite 12173-60-3, Illite 13918-37-1, Fayalite 14808-60-7, .alpha. **Quartz**, occurrence 17068-78-9, Anthophyllite 25666-97-1, Chrysolite
(study of ancient ceramics using XRF, XRD, thermal anal. and voltammetric techniques)

L87 ANSWER 3 OF 30 HCA COPYRIGHT 2003 ACS on STN

138:48256 Method and apparatus for tailoring an **etch** profile on semiconductor wafer. Fink, Steven (Tokyo Electron Limited, Japan). PCT Int. Appl. WO 2002101116 A1 20021219, 22 pp. DESIGNATED STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2002-US11900 20020606. PRIORITY: US 2001-PV296144 20010607.

AB An **etch** profile tailoring system for use with an **etching** process **carried** out on a **wafer**,

has a scavenging plate with a baseline **etch** profile, and at least one **etch** profile tuning structure such as a plug replaceably disposed with respect to the scavenging plate and configured to alter the baseline **etch** profile during the **etching** process. The scavenging plate is made preferably from **quartz**, carbon, or silicon. The method for performing maintenance on an **etch** profile tailoring system comprises the steps of performing an **etching** process on a wafer in accordance with a desired **etch** profile, detg. whether or not maintenance should be performed, and replacing with a second plug if needed before conducting the **etching** process on addnl. wafers.

IC ICM C23F001-02

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 56

ST semiconductor device fabrication **etching** profile

IT **Etching**
Semiconductor device fabrication
(method and app. for tailoring **etch** profile on semiconductor wafer)

IT 7440-21-3, Silicon, uses 7440-44-0, Carbon, uses 14808-60-7, **Quartz**, uses
(scavenging plate material; method and app. for tailoring **etch** profile on semiconductor wafer)

L87 ANSWER 4 OF 30 HCA COPYRIGHT 2003 ACS on STN

137:117823 **Etching** chamber with ring **holder** for decreasing polymer particle contamination in reactive plasma **etching** of semiconductor wafers. Huang, Yu Chih; Tsuei, Cherng Chang; Wu, I. Chang (Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan). U.S. US 6423175 B1 20020723, 6 pp. (English). CODEN: USXXAM. APPLICATION: US 1999-413654 19991006.

AB The dry-**etching** chamber for Si-semiconductor wafers is equipped with **wafer holder**, and with the assocd. focus ring (esp. **quartz**) used to confine plasma generated in the chamber onto the exposed wafer surface. The ring surface exposed to the chamber is microroughened to the depth of 1-10 .mu.m by sand blasting or chem. **etching** method. The roughened surface on the focus ring improves adhesion between polymeric film formed during the plasma **etching** process for sidewall passivation, and the surface of **quartz** focus ring, resulting in adherent polymer film that does not flake off to form contaminant particles on the **etched** wafer.

IT **7440-21-3, Silicon, processes**
(semiconductor, **etching** of; plasma-**etching** chamber with stable focus ring for decreased polymer particle contamination of semiconductor wafers)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C23F001-02
NCL 156345000
CC 76-2 (Electric Phenomena)
ST silicon wafer plasma **etching** focus ring stability
IT Semiconductor materials
(**etching** of; plasma-**etching** chamber with stable focus ring for decreased polymer particle contamination of semiconductor wafers)
IT **Etching**
(plasma, of semiconductor wafers; plasma-**etching** chamber with stable focus ring for decreased polymer particle contamination of semiconductor wafers)
IT 14808-60-7, **Quartz**, uses
(focus ring, in plasma **etching**; plasma-**etching** chamber with stable focus ring for decreased polymer particle contamination of semiconductor wafers)
IT **7440-21-3**, **Silicon**, **processes**
(semiconductor, **etching** of; plasma-**etching** chamber with stable focus ring for decreased polymer particle contamination of semiconductor wafers)

L87 ANSWER 5 OF 30 HCA COPYRIGHT 2003 ACS on STN
136:78230 Elimination/reduction of black silicon in DT **etch**.
Mathad, Gangadhara S.; Ranade, Rajiv (Infineon Technologies North America Corp., USA). PCT Int. Appl. WO 2001099159 A2 20011227, 13 pp. DESIGNATED STATES: W: JP, KR; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2001-US19659 20010620. PRIORITY: US 2000-597441 20000620.
AB In a method of **etching** a wafer in a plasma **etch** reactor, the improvement of conducting **etching** to reduce or eliminate black silicon comprising: (a) providing a plasma **etch** reactor comprising walls defining an **etch** chamber; (b) providing a plasma source chamber remote from and in communication with the **etch** chamber to provide a plasma to the **etch** chamber, and a **wafer chuck** or pedestal disposed in the **etch** chamber to seat a wafer; (c) providing a dielec. wall in proximity to and around a periphery of the wafer; (d) providing a modification to a lower Rf electrode by interposing conductor means into an extension of Vdc flat sheath boundary relation to the dielec. wall means and the wafer or in substitution for the dielec. wall; (e) forming a plasma within the plasma source chamber and providing the plasma to the **etch** chamber; and (f) supplying Rf energy to the **wafer chuck** to assist **etching** of the wafer by forming elec. fields between the upper surface of the wafer and the walls of the **etch** chamber, to provide extension of a Vdc flat sheath boundary beyond and into a defocusing relation to the wafer edge to reduce mask erosion and eliminate occurrence of black silicon formation.
IC ICM H01L021-00

CC 76-3 (Electric Phenomena)
ST integrated circuit black silicon elimination deep trench **etch**
IT Integrated circuits
Photomasks (lithographic masks)
Semiconductor device fabrication
Semiconductor devices
(elimination or redn. of black silicon in deep trench **etch** of semiconductor wafer in plasma reactor)
IT Borosilicate glasses
(elimination or redn. of black silicon in deep trench **etch** of semiconductor wafer in plasma reactor)
IT **Etching**
(plasma; elimination or redn. of black silicon in deep trench **etch** of semiconductor wafer in plasma reactor)
IT 7440-21-3P, Silicon, uses
(elimination or redn. of black silicon in deep trench **etch** of semiconductor wafer in plasma reactor)
IT 14808-60-7, **Quartz**, uses
(elimination or redn. of black silicon in deep trench **etch** of semiconductor wafer in plasma reactor)

L87 ANSWER 6 OF 30 HCA COPYRIGHT 2003 ACS on STN
135:337862 Apparatus for plasma **etching** of semiconductor wafers. Kanetani, Hiroyuki; Kumura, Yoshinori; Taniguchi, Yasuyuki; Kunishima, Iwao (Toshiba Corp., Japan). Jpn. Kokai Tokkyo Koho JP 2001308077 A2 20011102, 9 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2000-127952 20000427.
AB The app. contain electrostatic **chuck** mechanism housed in vacuum chambers, and **holding** semiconductor **wafers**, as well as covering which cover the wafer surroundings from above to prevent material dispersion and contamination.
IC ICM H01L021-3065
ICS C23C014-34; C23C014-50; H01L021-203; H01L027-105; H01L027-10
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 77
ST plasma **etching** app semiconductor wafer covering
IT Ferroelectric films
(app. for plasma **etching** to remove ferroelec. films on semiconductor wafers under coverings)
IT Magnetic materials
(app. for plasma **etching** to remove magnetic materials on semiconductor wafers under coverings)
IT Contamination (electronics)
(app. for plasma **etching** to remove magnetic materials on semiconductor wafers under coverings for prevention of)
IT **Etching** apparatus
Semiconductor device fabrication
(app. for plasma **etching** to surface treat semiconductor wafers under coverings)
IT **Etching**
(plasma; app. for plasma **etching** to surface treat

semiconductor wafers under coverings)

IT 409-21-2, Silicon carbide, uses 1344-28-1, Alumina, uses 7440-21-3, Silicon, uses 14808-60-7, **Quartz**, uses
(app. for plasma **etching** to surface treat semiconductor wafers under coverings coated with)

L87 ANSWER 7 OF 30 HCA COPYRIGHT 2003 ACS on STN

135:337827 Semiconductor device fabrication method during which characteristics are screened by reducing ground electrode inductance. Shimada, Masao (Nec Corporation, Japan). U.S. Pat. Appl. Publ. US 20010034081 A1 20011025, 14 pp. (English). CODEN: USXXCO. APPLICATION: US 2001-840578 20010423. PRIORITY: JP 2000-124721 20000425.

AB The present invention relates to a method of manufg. a semiconductor device. In particular, the present invention relates to a method of manufg. a semiconductor device by which characteristics of a semiconductor device can be evaluated in a wafer state. A surface of a semiconductor wafer having a plurality of semiconductor elements thereon is laminated on a 1st **wafer holding** substrate. Subsequently, the whole rear surface of the semiconductor wafer is coated with a 1st conductive layer. Then a 2nd conductive layer is selectively formed thereon. Then, a rear surface side glass substrate is laminated on the 1st and 2nd conductive layer. Subsequently, the 1st **wafer holding** substrate is peeled off. Subsequently, the semiconductor wafer is selectively **etched** so as to be sepd. into semiconductor elements. Then, the 1st conductive layer is connected to a ground potential to measure elec. characteristics of the semiconductor elements and sort the semiconductor elements into non-defectives and defectives. Then, the 1st conductive layer is selectively **etched** so as to be sepd. into chips and thus semiconductor pellets are formed. Finally, the 2nd **wafer holding** substrate is peeled off.

IC H01L021-44; H01L021-48; H01L021-50; H01L021-301; H01L021-46; H01L021-78

NCL 438114000

CC 76-3 (Electric Phenomena)

IT **Etching**
(selective; semiconductor device fabrication method during which characteristics are screened by reducing ground electrode inductance)

IT Electrically conductive pastes
Field effect transistors
Glass substrates
Lamination
Semiconductor device fabrication
(semiconductor device fabrication method during which characteristics are screened by reducing ground electrode inductance)

IT 1344-28-1, Alumina, uses 14808-60-7, **Quartz**, uses
(semiconductor device fabrication method during which characteristics are screened by reducing ground electrode

inductance)

L87 ANSWER 8 OF 30 HCA COPYRIGHT 2003 ACS on STN
135:234804 Semiconductor substrate, semiconductor device, its manufacture, and film-forming **jigs**. Abe, Hisashi (Sanyo Electric Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2001250775 A2 20010914, 9 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2000-59886 20000306.

AB The semiconductor substrate has a single crystal semiconductor film (A) formed by modifying a non-crystal semiconductor film (B) on .gtoreq.1 main surface of a dielec. substrate (C) such as a glass or **quartz**. The process involves (i) forming B on .gtoreq.1 main surface of C, (ii) bringing B into contact with a single crystal semiconductor (D), and (iii) irradiating electromagnetic wave, preferably laser, to the contacting area to modify B to C by using D as a seed crystal. The substrate is esp. suitable for semiconductor device such as TFT for a display or an image sensor. The **jigs** are shelves used for film-forming on 1 main plain of a substrate and are assembled with a plurality of supporting rods and the rod-supported racks whereupon the other side of the substrate is laid in close face-to-face contact with each other to avoid film deposition on the contacting surface. The **jig** is esp. suitable for forming an a-Si or poly-Si film on **quartz** substrate by low pressure CVD, or for forming a gate insulator or doped poly-Si film.

IT **7440-21-3, Silicon, processes**
(single crystal, conversion from non-crystal by laser irradn.; manuf. of semiconductor substrate for TFT and CVD **jigs** thereof)

RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L021-20
ICS C23C016-56; H01L021-205; H01L029-786; H01L021-336
CC 76-3 (Electric Phenomena)
IT Laser radiation
(conversion of non-crystal semiconductor film to single crystal by irradn. of; manuf. of semiconductor substrate for TFT and CVD **jigs** thereof)
IT **Jigs**
Semiconductor device fabrication
Thin film transistors
Vapor deposition apparatus
(manuf. of semiconductor substrate for TFT and CVD **jigs** thereof)
IT **7440-21-3, Silicon, processes**
(single crystal, conversion from non-crystal by laser irradn.; manuf. of semiconductor substrate for TFT and CVD **jigs** thereof)

IT 14808-60-7, **Quartz**, uses
(**substrate**, single crystal **Si** film on; manuf. of semiconductor substrate for TFT and CVD **jigs** thereof)

L87 ANSWER 9 OF 30 HCA COPYRIGHT 2003 ACS on STN
135:156585 **Quartz** coil springs and their manufacture. Imai, Masato; Onodera, Shinji; Yamada, Hiroshi (Super Cilicone Kenkyusho K. K., Japan). Jpn. Kokai Tokkyo Koho JP 2001221269 A2 20010817, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 2000-29003 20000207.
AB Coil springs made of **quartz** are claimed. The coil springs are manufd. by (a) placing a mandrel longer than the manufg. springs in a **quartz** tube and filling the space in the tube with a wax, (b) cutting the tube, along with the wax, with a machining disk placed at the tip of the mandrel into a prefixed spiral shape, (c) heating the spiral coil for melt removal of the wax and releasing the mandrel, and (d) treatment of the **quartz** spiral coil in HF for its **etching** to a desired thickness. The springs are suitable for use as **holders** in semiconductor **wafer** treatment furnaces, etc.
IC ICM F16F001-02
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** coil spring semiconductor **wafer** **holder**; spiral machining wax filled **quartz** tube
IT **Semiconductor device fabrication**
(coil springs used in; manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT Springs (mechanical)
(coil; manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT **Etching**
Machining
(manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT Waxes
(manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT Pipes and Tubes
(**quartz** glass; manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT 7664-39-3, Hydrofluoric acid, uses
(**etchant**; manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)
IT 60676-86-0, **quartz** glass

(manuf. of **quartz** coil springs by spiral machining of **quartz** tubes filled with wax followed by removal of wax and **etching**)

L87 ANSWER 10 OF 30 HCA COPYRIGHT 2003 ACS on STN
135:84112 Light emitting diodes with permanent substrates of transparent glass or **quartz** and their fabrication. Chang, Kuo-hsiung; Lin, Kun-chuan; Horng, Ray-hua; Huang, Man-fang; Wuu, Dong-sing; Wei, Sun-chin; Chen, Lung-chien (Visual Photonics Epitaxy Co., Ltd., Taiwan). U.S. US 6258699 B1 20010710, 12 pp. (English). CODEN: USXXAM. APPLICATION: US 1999-307681 19990510.
AB Light-emitting diode (LED) fabrication is described entailing the steps of growing light emitting regions on temporary substrates, bonding transparent substrates of glass or **quartz** to the light emitting regions and removing the temporary substrates. Metal bonding agents also serving as ohmic contact layers for the LED are used to bond the transparent substrates to form dual substrate LED elements which are heated in **wafer holding** devices that include graphite lower chambers and graphite upper covers with stainless steel screws. Because of the different thermal expansion coeffs. of stainless steel and graphite, the stainless steel screws apply pressures to the dual substrate LED elements during the heating process to assist the bonding of the transparent substrate.
IC ICM H01L021-30
NCL 438458000
CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76
ST light emitting diode transparent glass **quartz** substrate fabrication; LED transparent glass **quartz** substrate fabrication; thermal expansion induced compression LED fabrication
IT Electroluminescent devices
Semiconductor device fabrication
(light-emitting diodes with permanent substrates of transparent glasses or silica and their fabrication using thermal expansion-induced compression for bonding)
IT 22831-42-1, Aluminum arsenide (AlAs) 106312-00-9, Gallium indium phosphide 142586-29-6, Aluminum gallium arsenide (Al0.1-0.8Ga0.2-0.9As)
(light-emitting diodes with permanent substrates of transparent glasses or silica with **etching** stop layers of)
IT 7631-86-9, Silica, uses
(**quartz** form; light-emitting diodes with permanent substrates of transparent glasses or silica and their fabrication using thermal expansion-induced compression for bonding)

L87 ANSWER 11 OF 30 HCA COPYRIGHT 2003 ACS on STN
135:78714 Cleaning of reaction tubes for deposition and **etching** of silicon and titanium nitride. Nishimura, Kazuaki; Yamamoto, Hiroyuki; Spaul, Philip (Tokyo Electron, Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2001185489 A2 20010706, 7 pp. (Japanese). CODEN:

JKXXAF. APPLICATION: JP 1999-364382 19991222.
AB Reaction tubes, for deposition and dry **etching** of Si films or Ti nitride films, are cleaned by feeding chlorine gas for **etch** removal of Si deposited on the tube walls. **Quartz** tubes and **wafer boats** are not damaged by the cleaning process.
IT **7440-21-3, Silicon, processes**
(**etch** removal of Si and TiN deposited on reaction tubes for film deposition and **etching** by treatment with chlorine)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L021-205
ICS H01L021-3065; H01L021-304
CC 47-10 (Apparatus and Plant Equipment)
Section cross-reference(s): 76
ST cleaning reaction tube silicon deposition; chlorine gas **etching** reaction tube cleaning; titanium nitride deposition tube cleaning
IT Cleaning
Etching
Vapor deposition process
(**etch** removal of Si and TiN deposited on reaction tubes for film deposition and **etching** by treatment with chlorine)
IT **7440-21-3, Silicon, processes**
7782-50-5, Chlorine, processes 25583-20-4, Titanium nitride
(**etch** removal of Si and TiN deposited on reaction tubes for film deposition and **etching** by treatment with chlorine)

L87 ANSWER 12 OF 30 HCA COPYRIGHT 2003 ACS on STN
133:67008 **Jigs** for manufacture of **quartz** boats for semiconductor **wafers**. Yohkaichiya, Motoo; Sato, Kenichi; Sagae, Atsushi; Watabe, Yasuyuki; Ohshima, Yasutake (Toshiba Ceramics Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2000173943 A2 20000623, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-346047 19981204.
AB The **jigs** have guide grooves formed in **jig** supports , and are capable of precision fabrication of **quartz** boats without modification.
IC ICM H01L021-22
ICS H01L021-68
CC 76-3 (Electric Phenomena)
ST **quartz** boat **jig** semiconductor **wafer**
IT **Jigs**
(for manuf. of **quartz** boats for semiconductor **wafers**)

IT **Semiconductor device fabrication**
(**jigs** for manuf. of **quartz** boats for semiconductor **wafers**)
IT 14808-60-7, **Quartz**, uses
(**jigs** for manuf. of **quartz** boats for semiconductor **wafers**)

L87 ANSWER 13 OF 30 HCA COPYRIGHT 2003 ACS on STN
132:86743 High-purity **quartz** glass grooved **jig** for a **Si** semiconductor **wafer** heat processing apparatus and fabrication thereof. Ohashi, Nobuo; Yamagata, Shigeru (Shin-Etsu Quartz Products Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 2000021888 A2 20000121, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-198133 19980630.
AB The invention relates to a **quartz** glass grooved **jig** for high-purity **Si** semiconductor **wafer** heat processing app., i.e., a **wafer** boat, wherein the groove planes have an av. surface roughness 0.5-5 .mu.m.
IC ICM H01L021-324
ICS H01L021-22
CC 76-3 (Electric Phenomena)
ST **quartz** glass groove **silicon wafer** boat heat processing app
IT Combustion
(boats; high-purity **quartz** glass grooved **jig** for **Si** semiconductor **wafer** heat processing app.)
IT Electric furnaces
(heat-treatment; high-purity **quartz** glass grooved **jig** for **Si** semiconductor **wafer** heat processing app.)
IT **Semiconductor device fabrication**
(high-purity **quartz** glass grooved **jig** for **Si** semiconductor **wafer** heat processing app.)
IT 14808-60-7, **Quartz**, uses
(high-purity **quartz** glass grooved **jig** for **Si** semiconductor **wafer** heat processing app.)
IT 7440-21-3, Silicon, uses
(high-purity **quartz** glass grooved **jig** for **Si** semiconductor **wafer** heat processing app.)

L87 ANSWER 14 OF 30 HCA COPYRIGHT 2003 ACS on STN
132:72310 Screening of semiconductor **wafer jigs**. Matsuda, Satoshi; Kondo, Kazuyoshi; Abe, Emiko (Nippon Sekiei Glass K. K., Japan). Jpn. Kokai Tokkyo Koho JP 2000012669 A2 20000114, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-171732 19980618.
AB The invention relates to a process for screening semiconductor **wafer jigs** for particulate contaminants, wherein the **quartz jig** sample is subjected to ultrasonic vibration in pure H2O to release particles from microcracks for counting.

IC ICM H01L021-68
ICS G01N015-00; G06M011-00
CC 76-3 (Electric Phenomena)
ST semiconductor **wafer quartz jig** particulate contaminant
IT Holders
Semiconductor device fabrication
(screening of semiconductor **wafer jigs** for particulate contaminant)
IT 14808-60-7, **Quartz**, processes
(screening of semiconductor **wafer jigs** for particulate contaminant)

L87 ANSWER 15 OF 30 HCA COPYRIGHT 2003 ACS on STN
130:176211 **Wafer** support **jigs** for heat treatment apparatus. Shimizu, Hirofumi; Isomae, Seiichi; Suzuki, Tadashi; Minowa, Kyoko; Sato, Tomomi; Saito, Shigeaki; Natsuaki, Nobuyoshi; Kawamura, Masao (Hitachi, Ltd., Japan; Hitachi Cho LSI System Co., Ltd.). Jpn. Kokai Tokkyo Koho JP 11054447 A2 19990226 Heisei, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-211455 19970806.
AB The **jigs** are vertical boats to horizontally support **Si wafers** in heat treatment. The **jigs** are made of made of such materials as **quartz**, which are highly pure and have excellent thermal and corrosion resistance, as well as precision processing characteristic, and also have similar thermal expansion rate as the **Si wafers**.
IT **7440-21-3, Silicon, processes**
(**wafer** support **jigs** for heat treatment app.)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L021-22
ICS H01L021-22; H01L021-31; H01L021-68
CC 76-3 (Electric Phenomena)
ST **silicon wafer jig** heat treatment app; **quartz jig silicon wafer** heat treatment
IT Heat treatment
Jigs
Semiconductor materials
(**wafer** support **jigs** for heat treatment app.)
IT 14808-60-7, **Quartz**, uses
(**wafer** support **jigs** for heat treatment app.)
IT **7440-21-3, Silicon, processes**
(**wafer** support **jigs** for heat treatment app.)

L87 ANSWER 16 OF 30 HCA COPYRIGHT 2003 ACS on STN
130:102687 Manufacture of optical waveguides. Makikawa, Shinji; Ejima, Masatake; Konishi, Shigeru; Kamiya, Kazuo (Shin-Etsu Chemical

Industry Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 11002736 A2 19990106 Heisei, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-153211 19970611.

AB The manufg. process comprises a step of forming a **quartz** layer on a **Si** single crystal **substrate** by flame spray coating, where the av. particle diam. of the deposited **quartz** is <600.ANG.; and the av. surface roughness of the **quartz** layer is <50.ANG..

IC ICM G02B006-13

CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

ST optical waveguide **quartz** flame deposition silicon

IT Coating **process**
(**flame**-spraying; manuf. of optical waveguides)

L87 ANSWER 17 OF 30 HCA COPYRIGHT 2003 ACS on STN

129:223604 **Quartz** CVD **jig**, its manufacture, and semiconductor device fabrication using the **jig**. Fujii, Hiyoshiro; Kobayashi, Kazuo; Horie, Yasuhiko; Ohnishi, Hiroshi; Mimura, Seiichi (Mitsubishi Electric Corp., Japan). Jpn. Kokai Tokkyo Koho JP 10256161 A2 19980925 Heisei, 14 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-70824 19970307.

AB A **quartz** CVD **jig** for exposing a semiconductor **wafer** to a desired atm. has a hydroxide concn. .ltoreq.30 ppm at the surface for supporting the **wafer** to improve its resistance to a cleaning chem. Alternatively, the **jig** may have a film resistant a cleaning chem. A method for manufg. the **jig** is also described, together with semiconductor device fabrication using the **jig**.

IC ICM H01L021-205

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76

ST **quartz jig** CVD semiconductor device fabrication

IT Holders
Semiconductor device fabrication
Vapor deposition apparatus
(**quartz** CVD **jig** for semiconductor device fabrication)

IT 14808-60-7, **Quartz**, uses
(**quartz** CVD **jig** for semiconductor device fabrication)

L87 ANSWER 18 OF 30 HCA COPYRIGHT 2003 ACS on STN

127:350039 Process and apparatus for manufacture of **quartz** glass plates by vapor phase axial deposition (VAD). Ichinokura, Masato; Ishii, Tomoyuki; Tsuyuki, Tatsuya; Ikuno, Hiroto; Ishikawa, Yasuo (Toshiba Ceramics Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 09286621 A2 19971104 Heisei, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1996-122518 19960419.

AB The plates are manufd. by deposition of SiO2 soot formed by hydrolysis of raw Si compds. with oxyhydrogen **flame**, and the **process** esp. involves (1) depositing the soot layers

on a rotating roller, (2) peeling the layers having required thickness from the roller surface, and (3) sintering and vitrifying the resulting flat soot layers. The app. consists of (a) a main roller rotating to a certain direction, (b) a multitube burner placed in parallel with the rotating axis of the roller to form a fixed distance from the roller surface, to move back and forth between the both ends of the roller width, and to face its flame toward the roller surface for forming the soot, (c) a heating means which is placed to follow the roller rotated after contact with the tip of the burner flame and densify the soot layers on the roller, (d) a peeling means using a heater under the roller, (e) a sintering furnace for vitrifying the peeled soot layers, and (f) a conveyer for the resultant **quartz** glass. The plates for use in semiconductor **wafer** manuf. are directly and continuously obtained from the soot by the improved VAD method, whereas conventional methods via ingot forming process need a large amt. of energy and provide products polluted with impurities.

IC ICM C03B008-04
ICS C03B020-00
CC 57-1 (Ceramics)
ST **quartz** glass vapor phase axial deposition; silica soot VAD glass plate manuf
IT Flat glass
(**quartz** glass plate manuf. by vapor phase axial deposition)
IT 60676-86-0P, Silica, vitreous
(**quartz** glass plate manuf. by vapor phase axial deposition)

L87 ANSWER 19 OF 30 HCA COPYRIGHT 2003 ACS on STN
127:242094 Method for improving **etch** uniformity in remote source plasma reactors with powered **wafer chucks**
. Donohoe, Kevin G. (Micron Technology, Inc., USA). U.S. US 5662770 A 19970902, 9 pp. (English). CODEN: USXXAM. APPLICATION: US 1993-48991 19930416.
AB This invention is a hardware modification which permits greater uniformity of **etching** to be achieved in a high-d.-source plasma reactor (i.e., one which uses a remote source to generate a plasma, and which also uses high-frequency bias power on the **wafer chuck**). The invention addresses the uniformity problem which arises as the result of nonuniform power coupling between the wafer and the walls of the **etch** chamber. The soln. to greatly mitigate the nonuniformity problem is to increase the impedance between the wafer and the chamber walls. This may be accomplished by placing a cylindrical dielec. wall around the wafer. **Quartz** is a dielec. material that is ideal for the cylindrical wall if Si is to be **etched** selectively with respect to SiO2, since **quartz** is virtually inert under such conditions.
IT **7440-21-3, Silicon, processes**
(improving uniformity of plasma **etching** of)
RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L021-302
NCL 438716000
CC 76-11 (Electric Phenomena)
ST plasma **etching** uniformity improvement; silicon plasma **etching** uniformity improvement; dielec wall plasma **etching** reactor; **quartz** wall plasma **etching** reactor
IT Electric insulators
(improving uniformity of plasma **etching** using dielec. walls)
IT **Etching**
(plasma; improving uniformity of)
IT **Etching**
(selective; of silicon with respect to SiO_2)
IT **7440-21-3, Silicon, processes**
(improving uniformity of plasma **etching** of)
IT 14808-60-7, **Quartz**, uses
(improving uniformity of plasma **etching** using dielec. walls of)

L87 ANSWER 20 OF 30 HCA COPYRIGHT 2003 ACS on STN
125:236244 Doping silicon wafers using a solid dopant source and rapid thermal processing. Wolfe, John C.; Zagozdzon-Wosik, Wanda (The University of Houston System, USA). U.S. US 5550082 A 19960827, 7 pp., Cont. of U. S. Ser. No. 157,337, abandoned. (English). CODEN: USXXAM. APPLICATION: US 1995-414031 19950330. PRIORITY: US 1993-157337 19931118.
AB The present invention is, in part, a new process for dopant diffusion, both p-type (e.g., B) and n-type (e.g., P, As), into Si wafers, using rapid thermal processing (RTP). It uses a surface layer of a new planar dopant as an active dopant source. Such a source is produced using either a rigid **holder wafer** with a spin-on dopant or CVD doped oxide deposited on its surface, or such a source is a high-pressure planar solid source having a surface that has been activated by dry or sputter **etching**. Such a dopant source is placed in proximity to a **processed Si** wafer in such a manner that its active surface is facing the surface of the Si wafer during RTP. Both the Si wafer and the dopant source are heated by lamps emitting light causing transport of dopant from the dopant source to the Si surface. The dopant source may be produced using either Si wafers, **quartz** or ceramic plates, or planar solid diffusion sources which are com. available in a form of solid disks contg. compds. comprising various dopant atoms (e.g., B, P, and As).
IT **7440-21-3, Silicon, processes**
(doping **silicon** wafers using a solid dopant source and rapid thermal processing)

RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L021-223
NCL 437168000
CC 76-3 (Electric Phenomena)
ST doping silicon wafer solid dopant source; rapid thermal **processing** doping **silicon** wafer
IT Sputtering
(**etching**, in activation of solid dopant sources for doping silicon wafers)
IT **Etching**
(sputter, in activation of solid dopant sources for doping silicon wafers)
IT **7440-21-3, Silicon, processes**
(doping **silicon** wafers using a solid dopant source and rapid thermal processing)
IT 14808-60-7, **Quartz**, uses
(sources for doping silicon wafers based on plates of)

L87 ANSWER 21 OF 30 HCA COPYRIGHT 2003 ACS on STN
124:35610 **Quartz** glass tubes and their manufacture. Hayashi, Shigetoshi; Arahori, Tadahisa (Sumitomo Metal Ind, Japan). Jpn. Kokai Tokkyo Koho JP 07267661 A2 19951017 Heisei, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1994-55619 19940325.
AB The **quartz** glass tubes consist of a **quartz** glass internal layer with thickness .gtoreq.500.mu.m, and an outer **quartz** glass layer contg. 3-100 ppm Al with thickness .gtoreq.50% of the total thickness. The tubes are manufd. by: forming a porous **quartz** glass, adhering an Al compd. on the internal part of the porous glass, vitrifying by heating, forming a tube therewith, and forming an internal **quartz** glass layer. The tubes are esp. suitable for heat treating high-purity semiconductor material such as **Si wafer**.
IC ICM C03B020-00
ICS C03C003-06
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** glass tube manuf; semiconductor heat treatment **quartz** tube
IT **Firing**, heat-**treating process**
Pipes and Tubes
Semiconductor materials
(in manuf. of **quartz** glass tubes for heat treating of high-purity semiconductor materials)
IT 7429-90-5, Aluminum, uses
(in manuf. of **quartz** glass tubes for heat treating of high-purity semiconductor materials)

IT 60676-86-0, **Quartz** glass
(manuf. of **quartz** glass tubes for heat treating of high-purity semiconductor materials)

L87 ANSWER 22 OF 30 HCA COPYRIGHT 2003 ACS on STN
122:325076 Crystal structures and optical properties of tungsten oxide films prepared by a complexing-agent-assisted sol-gel process. Nishide, Toshikazu; Mizukami, Fujio (Nissan Research Center, Nissan Motor Co., Ltd., 1, Natsushima, Yokosuka, Kanagawa, 237, Japan). Thin Solid Films, 259(2), 212-17 (English) 1995. CODEN: THSFAP. ISSN: 0040-6090. Publisher: Elsevier.

AB Tungsten oxide (WO3) films were prepd. by the sol-gel process, using 2,4-pentanedione (PTN) as an org. ligand. The effect of the ligand on the crystn. and crystal structure of the WO3 films was examd. by Raman, IR and x-ray diffraction spectroscopies, and their optical properties were investigated in relation to the refractive index. Tungsten oxides prepd. with PTN on a **quartz** glass **substrate** and a **silicon wafer**, and those prepd. without PTN on a **silicon wafer** are amorphous when fired at 300.degree.C. The oxides crystd. when fired at temps. between 300 and 500.degree.C, and the amts. of cryst. WO3 increased when the films were fired at 700.degree.C. Only cubic crystals of WO3 were formed selectively on the **quartz** glass substrates when the films prepd. with PTN were fired at 500 and 700.degree.C. However, without PTN, a mixt. of cubic and monoclinic crystals was formed under the same **firing conditions**. The WO3 film prepd. with PTN and fired at 500.degree.C showed a lower value for the real part of the complex refractive index than that for the corresponding film prepd. without PTN. The WO3 film prepd. with PTN did not densify immediately after being fired, resulting in a lower value for the real part of the refractive index.

CC 73-2 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 75

L87 ANSWER 23 OF 30 HCA COPYRIGHT 2003 ACS on STN
120:285947 Parts for heat treatment of semiconductor **wafers** and manufacture thereof. Ito, Hironori; Iwanaka, Masafumi; Tsuyuki, Tatsuya; Ueshima, Nobuyuki (Toshiba Ceramics Co, Japan). Jpn. Kokai Tokkyo Koho JP 05254859 A2 19931005 Heisei, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1992-53515 19920312.

AB The part is made of synthetic **quartz** .ltoreq.20 ppm each in OH and Cl concn., and .gtoreq.1013 P in viscosity. The title process comprises formation of porous glass forms 0.4-0.6 g/cm3 in sp.gr. and .gtoreq.0.4 .mu.m in av. particle diam. of glass particles by hydrolysis of SiCl4 in an oxyhydrogen **flame** and heat **treatment** of the forms at 1000-1500.degree. in a H2 atm.

IC ICM C03B020-00
ICS H01L021-22; H01L021-324; H01L021-68

CC 75-3 (Crystallography and Liquid Crystals)

Section cross-reference(s): 57
ST synthetic **quartz** part annealing semiconductor
IT Annealing
(of semiconductor **wafers**, synthetic **quartz** parts for)
IT 7631-86-9P, Silica, preparation
(prepn. of synthetic **quartz**, parts from, for annealing of semiconductor **wafers**)

L87 ANSWER 24 OF 30 HCA COPYRIGHT 2003 ACS on STN
117:181445 Manufacture of **quartz** optical waveguides. Ito, Masumi; Kanamori, Hiroo; Ishikawa, Shinji; Aikawa, Haruhiko; Hoshino, Sumio (Sumitomo Electric Industries, Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 04131809 A2 19920506 Heisei, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1990-251880 19900925.
AB The manufg. process typically comprises the steps of: forming a **quartz** buffer layer (I) on a **Si wafer**; forming a glass ridge waveguide stripe (II) using a mask and a sputtering method; forming a glass cladding/burying layer (III); wherein I and III are formed by flame-hydrolysis deposition; and II contains a rare-earth dopant or semiconductor microparticles for a laser excitation or a nonlinear optical conversion, resp. The process produces versatile electrooptical elements with a high throughputs.
IC ICM G02B006-12
ICS G02F001-35; H01S003-07; H01S003-108
CC 73-12 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
ST nonlinear optical **quartz** waveguide manuf; laser amplifier **quartz** waveguide manuf; flame hydrolysis deposition **quartz** waveguide
IT Vapor deposition **processes**
(**flame** hydrolysis deposition, laser-amplifier/nonlinear **quartz** waveguides using)
IT Lasers
(**quartz** waveguide manuf. for)
IT Waveguides
(optical, laser-amplifier/nonlinear **quartz**, manuf. of)
IT 14808-60-7, **Quartz** (SiO_2), uses
(erbium or cadmium sulfide doped, buried waveguides from, by flame hydrolysis deposition)
IT 7440-21-3, Silicon, uses
(laser-amplifier/nonlinear **quartz** waveguides from, as substrate)

L87 ANSWER 25 OF 30 HCA COPYRIGHT 2003 ACS on STN
117:60762 Method and apparatus for doping silicon wafers using a solid dopant source and rapid thermal processing. Wolfe, John C.; Zagozdzon-Wosik, Wanda (University of Houston System, USA). PCT Int. Appl. WO 9205896 A1 19920416, 21 pp. DESIGNATED STATES: W: JP, KR; RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, NL, SE. (English). CODEN: PIXXD2. APPLICATION: WO 1991-US7333 19911002.

PRIORITY: US 1990-591791 19901002.
AB A new process for dopant diffusion, both p-type (e.g., B) and n-type (e.g., P, As), into Si-wafers, using rapid thermal processing (RTP) uses a surface layer of a new planar dopant as an active dopant source. Such a source is produced using either a rigid **holder wafer** with a spin-on dopant or CVD doped oxides deposited on its surface, or such a source is a high-pressure planar solid source having a surface that has been activated by dry **etching** or sputtering **etching**. Such a dopant source is placed in proximity to a **processed Si** wafer in such a manner that its active surface is facing the surface of the Si wafer during RTP. Both the Si wafer and the dopant source are heated by lamps emitting light causing transport of dopant from the dopant source to the Si surface. The dopant source may be produced using either Si wafers, **quartz** or ceramic plates or planar solid diffusion sources which are com. available in a form of solid disks contg. compds. contg. various dopant atoms (e.g., B, P, and As).
IC ICM B21F041-00
ICS B32B009-00; H01L021-00
CC 76-3 (Electric Phenomena)

L87 ANSWER 26 OF 30 HCA COPYRIGHT 2003 ACS on STN
113:236486 Square, **quartz** glass tanks with **rounded corners**. Hiraizumi, Chiyokichi; Hirano, Kazuo (Shin-Etsu Quartz Products Co., Ltd., Yamagata, Japan). Jpn. Kokai Tokkyo Koho JP 02102141 A2 19900413 Heisei, 6 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1988-254871 19881012.
AB These tanks, useful for cleaning or chem. treating semiconductor **wafers**, etc., are manufd. from arc-shaped glass prepd. by cutting cylindrical tubes lengthwise, glass plates, at least part of which is bent, and glass plates, the width of which is smaller than that of each wall of the square tanks by assembling the glass materials and welding. The **rounded corners** are formed by the arc-shaped glass or curved glass plates.
IC ICM C03B023-20
ICS C03C027-10; H01L021-304
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST **quartz** glass square container tank
IT 60676-86-0P, Vitreous silica
(containers, square, manuf. of, for cleaning or chem. treatment of semiconductor **wafers**)

L87 ANSWER 27 OF 30 HCA COPYRIGHT 2003 ACS on STN
109:220955 A durable and deformation-free **jig** for **processing silicon wafers**. Odo, Takashi; Tanaka, Takashi; Yanai, Nobuharu (Toshiba Ceramics Co., Ltd., Japan; Toshiba Corp.). Jpn. Kokai Tokkyo Koho JP 63164312 A2 19880707 Showa, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1988-310261 19861226.
AB The **jig** comprises a (**Si**-impregnated) SiC

base, and a **quartz**-glass **wafer** support
which makes contact with the entire length of the base at least on 1
side and has grooves for supporting **wafers**.
IC ICM H01L021-22
ICS H01L021-68
CC 76-3 (Electric Phenomena)
ST **silicon** carbide **jig wafer** processing;
quartz glass **jig wafer** processing;
semiconductor **wafer** processing **jig**
IT Semiconductor devices
(**silicon wafers** for, **jigs** for
processing of)
IT 409-21-2, Silicon carbide, uses and miscellaneous 60676-86-0,
Vitreous silica
(**jigs**, for **processing** of **silicon**
wafers)
IT 7440-21-3, Silicon, uses and miscellaneous
(**wafers**, **jig** for processing of)

L87 ANSWER 28 OF 30 HCA COPYRIGHT 2003 ACS on STN
100:44048 **Jig** for heat treatment of semiconductor
wafers. (Hitachi, Ltd., Japan). Jpn. Kokai Tokkyo Koho JP
58165319 A2 19830930 Showa, 2 pp. (Japanese). CODEN: JKXXAF.
APPLICATION: JP 1982-47386 19820326.
AB **Jigs** with long life times and which do not contaminate
Si wafers with **quartz** during heating
consist of **quartz** cores covered with a layer of poly-Si
.gtoreq.3000 .ANG. thick.
IC H01L021-22; H01L021-31
CC 76-3 (Electric Phenomena)
ST **jig** silicon heating polysilicon coating
IT Semiconductor devices
(polysilicon coated **quartz jigs** for heat
treatment of silicon)
IT Furnaces, electric
(polysilicon-coated **quartz jigs** for
processing of **silicon wafers** in)
IT 14808-60-7, uses and miscellaneous
(**jigs** from, coated with polysilicon for heat processing
of semiconductor **wafers**)
IT 7440-21-3, uses and miscellaneous
(polycryst. coatings from, for **quartz jigs**
for heat processing of semiconductor **wafers**)

L87 ANSWER 29 OF 30 HCA COPYRIGHT 2003 ACS on STN
44:58368 Original Reference No. 44:11047i,11048b-e Preparation of
high-silica porous bodies at low temperatures. Kitaigorodskii, I.
I. (D. I. Mendeleev Chem.-Technol. Inst., Moscow). Doklady Akademii
Nauk SSSR, 64, 219-21 (Unavailable) 1949. CODEN: DANKAS. ISSN:
0002-3264.
AB Finely ground **quartz** glass (99.9% SiO_2) and a special
low-melting borosilicate glass were thoroughly mixed in various

ratios, moistened, shaped into 20 .times. 3-5-mm. **disks**, by using pressure of 60 kg./sq. cm., and fired at around 750.degree.. During firing, the borosilicate glass seps. into two vitreous phases which are intimately mixed but differ in chem. compn. and characteristics. One phase contains 95% SiO2 and 5% other oxides and is strongly acid-resistant; the other phase contains 10% SiO2 and 90% other oxides and dissolves easily in acids. The **disks** were treated in boiling 0.5 N HCl to remove the chemically unstable phase. The remaining porous bodies contained 96 to 98% SiO2, water absorption was 30% regardless of initial compn., apparent porosity was 37%, and true porosity was 45%. The **disks** withstood rapid cooling from 1350 to 18.degree. without visible changes; the softening point was above 1480.degree.. Compn. of borosilicate glass and **conditions** of **firing** are not given.

CC 19 (Glass, Clay Products, Refractories, and Enameled Metals)

IT Glass
  (borosilicate, sintered **disks** from **quartz** glass and)

IT Sintering
  (of borosilicate glass with **quartz** glass)

IT Filtering materials
  (silica sintered **disks**)

L87 ANSWER 30 OF 30 HCA COPYRIGHT 2003 ACS on STN

24:38842 Original Reference No. 24:4193i,4194a The power consumed by rotating **disks** and other shaped objects in fluid media. Fahrenwald, A. W.; Staley, W. W. Bur. Mines, Rept. of Investigations, 3006, 7 pp.,23 figs (Unavailable) 1930.

AB Of the factors considered, viscosity and density have the greatest influence on power consumption, being more or less directly proportional. The app. used was not sensitive enough to detect with certainty the differences caused by substances lowering surface tension. The impeller gave the greatest aeration with the blades set at 30.degree.. Results with a **quartz**-water pulp show that a pulp d. of 30-35% would be the most economical of power. Power consumption varied directly as the diam. of the **disk** . Thin **disks** used less power than thick, and knife-**edged** than **blunt**.

CC 2 (General and Physical Chemistry)

=> d l88 1-13 cbib abs hitstr hitind

L88 ANSWER 1 OF 13 HCA COPYRIGHT 2003 ACS on STN

138:213615 Method and apparatus for chemical-mechanical jet **etching** of Si, GaAs, glass and other semiconductor structures. Bachrach, Robert Z.; Chinn, Jeffrey D. (USA). U.S. Pat. Appl. Publ. US 2003038110 A1 20030227, 9 pp. (English). CODEN: USXXCO. APPLICATION: US 2001-932396 20010817.

AB A chem.-mech. jet **etching** method rapidly removes large amts. of material in **wafer** thinning, or produces

large-scale features on a **silicon wafer**, gallium arsenide substrate, or similar flat semiconductor workpiece, at **etch** rates in the range of 10-100 .mu. of workpiece thickness per min. A nozzle or array of nozzles, optionally including a dual-orifice nozzle, delivers a high-pressure jet of machining **etchant** fluid to the surface of the workpiece. The machining **etchant** comprises a liq. or gas, **carrying** a particulate material such as silica fine particles. The liq. may be a chem. **etchant**, or a solvent for a chem. **etchant**, selected from KOH, NaOH, HF, HNA (an aq. soln. of .apprx.7 wt.% HF, .apprx.30 wt.% HNO3, and .apprx.10 wt.% CH3COOH), TMAH (Tetramethylammonium Hydroxide), EDP (Ethylene Diamine Pyrochatechol), or amine gallates. The areas which are not to be **etched** may be shielded from the jet by a patterned mask, or the jet may be directed at areas from which material is to be removed, as in **wafer** thinning or direct writing, depending on the size of the desired feature or **etched** area.

IT **7440-21-3, Silicon, processes**
(**silicon wafer**, semiconductor **substrate**; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C03C015-00
ICS B44C001-22; C04B041-91; C23F001-00

NCL 216052000; 216092000; 216099000; 216097000; 216100000; 216101000

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57

ST silicon gallium arsenide silica glass semiconductor chem mech **etching**

IT **Semiconductor device fabrication**
(Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT **Etching**
(chem.-mech. jet **etching**; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT **Etching** masks
(patterned mask; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT Ceramics
(semiconductor substrate; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT Borosilicate glasses

Glass, processes
(semiconductor substrate; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT 149-91-7, Gallic acid, processes
(amines,chem. **etchant**; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT 64-19-7, Acetic acid, processes 75-59-2, Tetramethylammonium Hydroxide 1310-58-3, Potassium hydroxide (KOH), processes 1310-73-2, Sodium hydroxide (NaOH), processes 7664-39-3, Hydrofluoric acid, processes 7697-37-2, Nitric acid, processes 104048-99-9
(chem. **etchant**; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT 12033-89-5, Silicon nitride, uses
(**etching** mask; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT 7631-86-9, Silica, processes
(semiconductor substrate, **etching** particulate; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT 1303-00-0, Gallium arsenide, processes 14808-60-7, **Quartz**, processes
(semiconductor substrate; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

IT **7440-21-3**, **Silicon**, **processes**
(**silicon wafer**, semiconductor **substrate**; Method and app. for chem.-mech. jet **etching** of Si, GaAs, glass and other semiconductor structures)

L88 ANSWER 2 OF 13 HCA COPYRIGHT 2003 ACS on STN

136:94543 Semiconductor processing equipment having improved particle performance using ceramics. Bosch, William Frederick (Lam Research Corporation, USA). PCT Int. Appl. WO 2002003427 A2 20020110, 40 pp. DESIGNATED STATES: W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM; RW: AT, BE, BF, BJ, CF, CG, CH, CI, CM, CY, DE, DK, ES, FI, FR, GA, GB, GR, IE, IT, LU, MC, ML, MR, NE, NL, PT, SE, SN, TD, TG, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2001-US20284 20010625. PRIORITY: US 2000-607922 20000630.

AB A ceramic part having a surface exposed to the interior space, the surface having been shaped and plasma conditioned to reduce particles thereon by contacting the shaped surface with a high

intensity plasma. The ceramic part can be made by sintering or machining a chem. deposited material. During processing of semiconductor substrates, particle contamination can be minimized by the ceramic part as a result of the plasma conditioning treatment. The ceramic part can be made of various materials such as alumina, SiO2, **quartz**, C, Si, Si carbide, Si nitride, B nitride, B carbide, Al nitride or Ti carbide. The ceramic part can be various parts of a vacuum processing chamber such as a liner within a sidewall of the processing chamber, a gas distribution plate supplying the process gas to the processing chamber, a baffle plate of a showerhead assembly, a **wafer** passage insert, a focus ring surrounding the substrate, an edge ring surrounding an electrode, a plasma screen and/or a window.

IC ICM H01L021-00

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57

IT **Semiconductor device fabrication**
(app.; semiconductor processing equipment having improved particle performance using ceramics)

IT **Etching** apparatus
Reactors
(plasma; semiconductor processing equipment having improved particle performance using ceramics)

IT Electric discharge devices
Holders
Linings (refractory)
Machining
Sintering
Vacuum chambers
Windows
(semiconductor processing equipment having improved particle performance using ceramics)

IT 409-21-2, Silicon carbide SiC, uses 1344-28-1, Alumina, uses 7440-21-3, **Silicon**, uses 7440-44-0, Carbon, uses 7631-86-9, Silica, uses 7782-42-5, Graphite, uses 10043-11-5, Boron nitride, uses 12033-89-5, Silicon nitride, uses 12069-32-8, Boron carbide 12070-08-5, Titanium carbide 24304-00-5, Aluminum nitride
(semiconductor **processing** equipment having improved particle performance using ceramics)

L88 ANSWER 3 OF 13 HCA COPYRIGHT 2003 ACS on STN

134:319430 Field emission from carbon nanotubes grown by layer-by-layer deposition method using plasma chemical vapor deposition. Chung, S. J.; Hoon, S.; Jin Jang, L. (Department of Physics, Kyung Hee University, Dongdaemoon-ku, Seoul, 130-701, S. Korea). Thin Solid Films, 383(1,2), 73-77 (English) 2001. CODEN: THSFAP. ISSN: 0040-6090. Publisher: Elsevier Science S.A..

AB We developed a noble carbon nanotube (CNT) deposition method using a layer-by-layer technique, in which the deposition of a thin layer of CNTs and a CF4 plasma exposure on its surface were **carried** out alternatively. Owing to the difference in the **etch**

rate between amorphous carbon, graphite and CNTs by CF4 plasma, we can selectively **etch** out some of the unwanted amorphous carbon and graphite phases from the CNTs. In addn., CF4 plasma treatment on the surface can open the ends of the deposited CNTs and results in the increase of emission currents. The new CNTs exhibited a turn-on field of 1.2 V/.mu.m.

IT **7440-21-3, Silicon, processes**
(**substrate**; field emission from carbon nanotubes grown by layer-by-layer deposition method using plasma chem. vapor deposition)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

CC 76-12 (Electric Phenomena)

ST field emission carbon nanotube PECVD plasma **etching**

IT **Etching**
Vapor deposition process
(plasma; field emission from carbon nanotubes grown by layer-by-layer deposition method using plasma chem. vapor deposition)

IT 75-73-0, Tetrafluoromethane
(plasma, **etchant**; field emission from carbon nanotubes grown by layer-by-layer deposition method using plasma chem. vapor deposition)

IT **7440-21-3, Silicon, processes**
14808-60-7, **Quartz**, processes
(**substrate**; field emission from carbon nanotubes grown by layer-by-layer deposition method using plasma chem. vapor deposition)

L88 ANSWER 4 OF 13 HCA COPYRIGHT 2003 ACS on STN

134:64944 Apparatus for preventing plasma **etching** of a **wafer** clamp in semiconductor fabrication processes. Lu, Wen-Chuan; Lu, Chung-Chien; Chou, Chih-Houng; Lin, Gary (United Microelectronics Corp., Taiwan). U.S. US 6165276 A 20001226, 7 pp. (English). CODEN: USXXAM. APPLICATION: US 1999-398732 19990917.

AB An app. for preventing plasma **etching wafer** clamp is disclosed in a process chamber. The app. comprises a pedestal, a bottom electrode, a **wafer** clamp, a semiconductor **wafer**, a **quartz** ring, a top electrode, a cooling plate, a anodizer, and a gas hole. The **wafer** clamp was used to secure the semiconductor **wafer**. However, the **wafer** clamp includes a clamp ring, a concave **holder**, and a depression. The clamp ring was used to support the semiconductor **wafer**. The concave **holder** has a semi-elliptical surface, polymer being formed on the backside of the concave **holder** to prevent plasma **etching** in the deposition or **etching** process, into the clamp ring. Then the depression is moved to a higher position

adjacent the concave **holder**.
IC ICM C23C016-00
ICS C23C016-04
NCL 118728000
CC 76-3 (Electric Phenomena)
ST plasma **etching** app semiconductor **wafer** clamp
IT **Holders**
Semiconductor device fabrication
(app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT Anodization
(app.; in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT Plates
(cooling; in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT Electrodes
Nozzles
(in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT Polymers, processes
(in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT **Etching** apparatus
(plasma; app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT Cooling apparatus
(plates; in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)
IT 7631-86-9, Silica, uses
(ring; in app. for preventing plasma **etching** of **wafer** clamp in semiconductor fabrication processes)

L88 ANSWER 5 OF 13 HCA COPYRIGHT 2003 ACS on STN
133:98134 Process chamber with inner support for CVD and other processing of semiconductor **wafers**. Wengert, John F.; Jacobs, Loren R.; Halpin, Michael W.; Foster, Derrick W.; Vander Jeugd, Cornelius A.; Vyne, Robert M.; Hawkins, Mark R. (ASM America Inc., USA). U.S. US 6093252 A 20000725, 46 pp., Cont.-in-part of U. S. Ser. No. 549,461, abandoned. (English). CODEN: USXXAM. APPLICATION: US 1996-637616 19960425. PRIORITY: US 1995-PV1863 19950803; US 1995-549461 19951027.
AB An improved chem.-vapor deposition reaction chamber having an internal support plate to enable reduced pressure processing. The chamber has a vertical-lateral lenticular cross-section with a wide horizontal dimension and a shorter vertical dimension between bi-convex upper and lower walls. A central horizontal support plate is provided between two lateral side rails of the chamber. A large rounded rectangular aperture is formed in the support plate for positioning a rotatable susceptor on which a **wafer** is placed. The shaft of the susceptor extends downward through the aperture and through a lower tube depending from the chamber. The

support plate segregates the reaction chamber into an upper region and a lower region, with purge gas being introduced through the lower tube into the lower region to prevent unwanted deposition therein. A temp. compensation ring is provided surrounding the susceptor and supported by fingers connected to the support plate. The temp. compensation ring may be circular or may be built out to conform to the rounded rectangular shape of the support plate aperture. The ring may extend farther downstream from the susceptor than upstream. A sep. sacrificial **quartz** plate may be provided between the circular temp. compensation ring and the rounded rectangular aperture. The **quartz** plate may have a horizontal portion and a vertical lip in close abutment with the aperture to prevent devitrification of the support plate. A gas injector abuts an inlet flange of the chamber and injects process gas into the upper region and purge gas into the lower region. The gas injector includes a plurality of independently controlled channels disposed laterally across the chamber, the channels merging at an outlet of the injector to allow mixing of the adjacent longitudinal edges of the sep. flows well before reaching the **wafer**. The chamber may also be used for other processing, e.g., annealing, **etching**, plasma-enhanced deposition, etc.

IC ICM C23C016-00
NCL 118719000
CC 76-3 (Electric Phenomena)
ST process chamber inner support semiconductor **wafer**; CVD chamber inner support semiconductor **wafer**
IT Vapor deposition process
 (chem.; process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT Vapor deposition process
 (plasma; process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT Annealing
 Etching
 Semiconductor device fabrication
 (process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT **Holders**
 (support, inner; process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT Plates
 (support; process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT Semiconductor materials
 (**wafers**; process chamber with inner support for CVD and other processing of semiconductor **wafers**)
IT 14808-60-7, **Quartz**, uses 60676-86-0, Silica vitreous
 (chamber; process chamber with inner support for CVD and other processing of semiconductor **wafers**)

L88 ANSWER 6 OF 13 HCA
131:315746 Quality and performance of late Ga+ ion FIB mask repair with

the gas assist in DUV process. Bae, Sang-Man; Koo, Youngmo; Ko, Kwang-Yoon; Kim, Bong Ho; Ahn, Dong-Joon (Memory Prod. and Technol. Dev. Div., Hyundai Electronics Co., Ichon-kun, Kyoungki-do, S. Korea). Proceedings of SPIE-The International Society for Optical Engineering, 3679(Pt. 2, Optical Microlithography XII), 1009-1018 (English) 1999. CODEN: PSISDG. ISSN: 0277-786X. Publisher: SPIE-The International Society for Optical Engineering.

AB Photomask quality for the next generation processing such as DUV scanner lithog. is crit., but there still are many problems. In this situation, we have to find some keys to solve these problems to accommodate the narrow scope of the process margin and the printing bias control on **wafer**, as well as coarse lithog. margins. Currently, the CD uniformity of the patterned Cr, or PSM features including the repaired mask patterns, is about .+-.0.03um. In next generation photomask prodn., there are some fundamental difficulties to overcome. Firstly, there is the inherent phys. behavior of DUV laser on **quartz** substrate, and secondly, there are photomask, defects that invisible to blue laser inspection, but can still be portioned onto the **wafer**. In order to keep up with photomask product requirements, the next generation inspection systems are being developed with i-line and KrF laser sources. However, issues such as low-level transmission defects and crit. line-widths defects have not been solved yet. In part, the Ga+ implantation defect is one of these invisible transmission defects due to the fact that the **carried** inspection tools use a blue laser, so it is not counted as killing defect of the DUV transmitted types. Although it is captured into a false defect, we have a difficult to classify by ion implantation defect. This paper discusses the process margins of FIB Ga+ ion scanning on the opaque repairing of damaged **quartz** substrate. It will show the effects of reduced intensity or using the Gas Assisted **Etching** process. And though it has been solved somewhat, we also have to consider the CD control specifications for the next generation device such as 1G DRAM with DUV lithog. In this expt., we have evaluated the printability of 4X DUV scanner after both opaque and clear defect repair with a focused ion beam (FIB) system. We also confirmed the accuracy of edge repair, implantation effects of each FIB machine and detd. the topog. of repair by AFM.

IT **7440-21-3, Silicon, processes**
(quality and performance of late Ga+ ion FIB mask repair with the gas assist in DUV process)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): 76

IT **Etching**
(dry, gas-assisted; quality and performance of late Ga+ ion FIB

mask repair with the gas assist in DUV process)
IT Ion implantation
Photomasks (lithographic masks)
Semiconductor device fabrication
(quality and performance of late Ga+ ion FIB mask repair with the gas assist in DUV process)
IT **7440-21-3, Silicon, processes**
(quality and performance of late Ga+ ion FIB mask repair with the gas assist in DUV process)

L88 ANSWER 7 OF 13 HCA COPYRIGHT 2003 ACS on STN
130:360083 Production method of SOI **wafer** and SOI **wafer** itself. Abe, Takao; Nakazato, Yasuaki; Uchiyama, Atsuo; Yoshizawa, Katsuo (Shin-Etsu Handotai Co., Ltd., Japan; Nagano Electronics Industrial Co., Ltd.). Jpn. Kokai Tokkyo Koho JP 11145438 A2 19990528 Heisei, 7 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1997-329507 19971113.
AB A method for fabricating a SOI **wafer** having a uniform film thickness, good crystallinity, and high **carrier** mobility Si layer involves contacting a single-crystal **Si wafer** implanted with hydrogen or rare-gas ions to an insulator substrate at a room temp., heating at 100-300 .degree.C to pre-bond the **wafer** and substrate, **etching** the **wafer** with a base to form a Si layer having a thickness 100-250 .mu.m, heating at 350-500 .degree.C to effect bonding, polishing the Si layer to a thickness .ltoreq.50 .mu.m, heating to .gtoreq.500 .degree.C to cleave at the implanted layer and form a single-crystal Si layer .ltoreq.0.5 .mu.m, polishing the Si layer to form a mirror surface, and heating at .gtoreq.800 .degree.C to strengthen the bonding. Specifically, the substrate may comprise **quartz**, alumina, glass, Si nitride, Al nitride, or Si carbide.
IT **7440-21-3, Silicon, processes**
(SOI **wafer**)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L027-12
ICS H01L021-02; H01L021-306
CC 76-3 (Electric Phenomena)
ST SOI semiconductor **wafer etching** polishing ion implantation
IT Semiconductor materials
(SOI **wafer**; **etching**, polishing, heating in fabrication of)
IT **Etching**
(dry; in fabrication of SOI **wafer**)
IT Glass substrates
(fabrication of SOI **wafer** from)

IT **Etching**
Ion implantation
Polishing
(in fabrication of SOI **wafer**)
IT **7440-21-3, Silicon, processes**
(SOI **wafer**)
IT 409-21-2, **Silicon** monocarbide, **processes**
1344-28-1, Alumina, processes 12033-89-5, **Silicon**
nitride, **processes** 14808-60-7, **Quartz**,
processes 24304-00-5, Aluminum nitride
(fabrication of SOI **wafer** from)

L88 ANSWER 8 OF 13 HCA COPYRIGHT 2003 ACS on STN
130:360082 Production method of SOI **wafer** and SOI
wafer itself. Abe, Takao; Nakazato, Yasuaki; Uchiyama,
Atsuo; Yoshizawa, Katsuo (Shin-Etsu Handotai Co., Ltd., Japan;
Nagano Electronics Industrial Co., Ltd.). Jpn. Kokai Tokkyo Koho JP
11145437 A2 19990528 Heisei, 6 pp. (Japanese). CODEN: JKXXAF.
APPLICATION: JP 1997-329506 19971113.

AB A method for fabricating a SOI **wafer** having a uniform film thickness, good crystallinity, and high **carrier** mobility Si layer involves contacting a single-crystal **Si** **wafer** to an insulator substrate at a room temp., heating at 100-300 .degree.C to pre-bond the **wafer** and substrate, **etching** the **wafer** with a base to form a Si layer having a thickness 100-250 .mu.m, heating at 350-500 .degree.C to effect bonding, polishing the Si layer to a thickness 2-20 .mu.m, vapor-phase **etching** the Si layer to a thickness .ltoreq.0.5 .mu.m, and heating at .gtoreq.800 .degree.C to increase the bonding. Specifically, the substrate may comprise **quartz**, alumina, glass, Si nitride, Al nitride, or Si carbide.

IT **7440-21-3, Silicon, processes**
(SOI **wafer**)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM H01L027-12
ICS H01L021-02; H01L021-306
CC 76-3 (Electric Phenomena)
ST SOI semiconductor **wafer** **etching** polishing
IT Semiconductor materials
(SOI **wafer**; **etching**, polishing, heating in
fabrication of)
IT **Etching**
(dry; in fabrication of SOI **wafer**)
IT Glass substrates
(fabrication of SOI **wafer** from)
IT **Etching**

Polishing
(in fabrication of SOI **wafer**)
IT **7440-21-3, Silicon, processes**
(SOI **wafer**)
IT 409-21-2, **Silicon** monocarbide, **processes**
1344-28-1, Alumina, processes 12033-89-5, **Silicon** nitride, **processes** 14808-60-7, **Quartz**, processes 24304-00-5, Aluminum nitride
(fabrication of SOI **wafer** from)

L88 ANSWER 9 OF 13 HCA COPYRIGHT 2003 ACS on STN
129:155766 Removal of silicon-containing coatings obtained in low-pressure CVD. Schmalzbauer, Klaus; Eichinger, Andreas (Siemens A.-G., Germany). Ger. Offen. DE 19703204 A1 19980730, 4 pp. (German). CODEN: GWXXBX. APPLICATION: DE 1997-19703204 19970129.
AB The coatings of doped or undoped polycryst. Si and/or Si_3N_4 obtained on furnace **boats** of SiC or **quartz** used as a support in treatment of semiconductor **wafers** are removed by plasma **etching** with an **etchant** contg. O and .gtoreq.1 F-contg., compd. such as SF_6, $SiCl_4$, NF_3, and CF_4.
IT **7440-21-3, Silicon, processes**
(plasma **etching** for removal of silicon-contg. coatings obtained in low-pressure CVD)
RN 7440-21-3 HCA
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IC ICM C23F004-00
CC 76-14 (Electric Phenomena)
Section cross-reference(s): 57
ST silicon contg coating removal plasma **etching**; oxygen plasma **etching** silicon coating removal; fluoride plasma **etching** silicon coating removal
IT **Etching**
(plasma; in plasma **etching** for removal of silicon-contg. coatings obtained in low-pressure CVD)
IT 75-73-0, Carbon fluoride (CF_4) 2551-62-4, Sulfur fluoride (SF_6) 7782-44-7, Oxygen, processes 7783-54-2, Nitrogen fluoride (NF_3) 10026-04-7, Silicon chloride ($SiCl_4$)
(in plasma **etching** for removal of silicon-contg. coatings obtained in low-pressure CVD)
IT **7440-21-3, Silicon, processes**
12033-89-5, **Silicon** nitride (Si_3N_4), **processes**
(plasma **etching** for removal of silicon-contg. coatings obtained in low-pressure CVD)

L88 ANSWER 10 OF 13 HCA COPYRIGHT 2003 ACS on STN
123:355854 Ultrathin single-crystalline silicon on **quartz** (SOQ) by 150 .degree.C **wafer** bonding. Tong, Q.-Y.; Goesele, U.; Martini, T.; Reiche, M. (Wafer Bonding Laboratory,

School of Engineering, Duke University, Durham, NC, 27708-0300, USA). Sensors and Actuators, A: Physical, A48(2), 117-23 (English) 1995. CODEN: SAAPEB. ISSN: 0924-4247. Publisher: Elsevier.

AB Single-cryst. Si films with thicknesses as thin as 2000 .ANG. were prepd. on thermally mismatched **quartz** substrates by a simple **wafer**-bonding approach. Initial bonding at .apprxeq.80.degree., storage at room temp. for >100 h and multi-temp. (max. 150.degree.) consecutive annealing with a 1.degree. min-1 ramping rate were adopted to strengthen the bond and to prevent debonding at the edge of the bonded pairs during annealing and **etching**, where thermal shearing and peeling stresses are max. Final **etching** by EDP (ethylenediamine-pyrocatechol-H2O) effectively reduces the peeling failure of the highly stressed thinned Si layer, mainly due to a reduced lateral oxide **etching** rate along the interface. The high **carrier** mobility in the single-cryst. Si layer and the transparent and insulating **quartz** substrate provides a new dimension of freedom in applications.

IT **7440-21-3, Silicon, processes**
(ultrathin single-cryst. silicon on **quartz** by 150.degree.C **wafer** bonding affected by annealing and **etching**)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

CC 76-3 (Electric Phenomena)

ST ultrathin cryst silicon **quartz** bonding; SOQ bonding annealing

IT Interface
(bonding; ultrathin single-cryst. silicon on **quartz** by 150.degree.C **wafer** bonding affected by annealing and **etching**)

IT Annealing
Etching
(ultrathin single-cryst. silicon on **quartz** by 150.degree.C **wafer** bonding affected by annealing and **etching**)

IT 107-15-3, Ethylenediamine, uses 120-80-9, Pyrocatechol, uses 1310-58-3, Potassium hydroxide, uses
(ultrathin single-cryst. silicon on **quartz** (SOQ) by 150 .degree.C **wafer** bonding affected by **etching** in soln. contg.)

IT **7440-21-3, Silicon, processes**
14808-60-7, **Quartz**, processes
(ultrathin single-cryst. silicon on **quartz** by 150.degree.C **wafer** bonding affected by annealing and **etching**)

L88 ANSWER 11 OF 13 HCA COPYRIGHT 2003 ACS on STN

123:129502 Measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma: study was SiO2 selective **etching** kinetics. Kubota, Kazuhiro; Matsumoto, Hiroyuki; Shindo, Haruo; Shingubara, Shoso; Horike, Yasuhiro (Dep. Elec. Eng., Toyo Univ., Kawagoe, 350, Japan). Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers, 34(4B), 2119-24 (English) 1995. CODEN: JAPNDE. ISSN: 0021-4922. Publisher: Japanese Journal of Applied Physics.

AB The kinetics of highly selective SiO2 **etching** were studied from appearance mass spectroscopy (AMS) measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma (ICP). Results obtained by varying of H2 concn. in C4F8, total pressure and RF power implied that CF1 radical played a major role in the polymer film deposition. In particular, radical measurements **carried** out by varying the length of a **quartz** tube which was set in front of an inlet of radicals effusing into AMS revealed that CF2 radical might not contribute to the polymer deposition and that the sticking probability of CF1 radical was reduced considerably in the presence of H. Also in the **etching** using a capillary plate as a high-aspect-ratio mask, the C-rich polymer film is deposited on the **Si** bottom **surface** in the presence of H at high CF1/CF2 radical d. ratio. Accordingly, CF1 radicals whose surface loss is suppressed in the presence of H probably arrive at deep the bottom surface, forming the C-rich polymer by reaction of H with F from CF1 radicals.

IT **7440-21-3, Silicon, processes**
(plasma **etching** kinetics of Si and SiO2 by C4F8/H2)

RN 7440-21-3 HCA

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

CC 76-11 (Electric Phenomena)

ST perfluorocyclobutane hydrogen plasma **etching** silica; fluorocarbon radical plasma **etching** silica

IT Sputtering
(**etching**, measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma **etching** of SiO2)

IT **Etching**
(sputter, measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma **etching** of SiO2)

IT Kinetics of **etching**
(sputter, plasma **etching** kinetics of Si and SiO2 by C4F8/H2)

IT 115-25-3, Perfluorocyclobutane
(measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma **etching** of SiO2)

IT 2154-59-8, Carbon fluoride (CF2) 2264-21-3, Carbon fluoride (CF3) 3889-75-6, Carbon fluoride (CF)

(measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma **etching** of SiO2)

IT 1333-74-0, Hydrogen, processes 7631-86-9, Silica, processes
(measurement of fluorocarbon radicals generated from C4F8/H2 inductively coupled plasma **etching** of SiO2)

IT **7440-21-3, Silicon, processes**
(plasma **etching** kinetics of Si and SiO2 by C4F8/H2)

L88 ANSWER 12 OF 13 HCA COPYRIGHT 2003 ACS on STN

120:257686 High quality silicon epitaxy in an ultra high vacuum rapid thermal CVD reactor: an application to single **wafer** processing. Sanganeria, Mahesh K.; Violette, Katherine E.; Ozturk, Mehmet C. (Dep. Electr. Comput. Eng., North Carolina State Univ., Raleigh, NC, 27695-7911, USA). Materials Research Society Symposium Proceedings, 303(Rapid Thermal and Integrated Processing II), 25-30 (English) 1993. CODEN: MRSPDH. ISSN: 0272-9172.

AB The authors report epitaxial growth of Si in an ultra high vacuum rapid thermal CVD (UHV/RTCVD) equipment. The objectives were low temp./low thermal budget processing and a high throughput compatible with single **wafer** manufg. The reactor consists of a load lock, a main process chamber and an intermediate cryo-pumped vacuum buffer chamber between the 2 chambers. An ultra-clean process environment was achieved using oil free pumps and point of use gas purifiers. The **wafer** is heated by a Peak Systems LXU-35 arc lamp through a **quartz** window. In this system, the authors achieved good quality Si epitaxy at low temp. (T .ltoreq. 800.degree.) in the very low, 100 mTorr, pressure regime with high throughput (Growth rate>0.25 .mu.m/min.). High growth rate was achieved using Si2H6 as the reactant gas instead of SiH4 or SiH2Cl2 which are more commonly used gases for epitaxial growth. High temp. in-situ cleaning was completely eliminated by initiating film growth on a H passivated surface obtained via dil. HF **etching**. Generation lifetimes in the 200-400 .mu.s range were measured for deposition temps. of 700.degree., 750.degree. and 800.degree. with no strong dependence on the deposition temp.

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76

ST VPE **silicon** single **wafer processing**

IT Electric current **carriers**
(lifetime of, effect of silicon epitaxial growth conditions on)

IT Passivation
(of silicon with hydrogen by **etching** for VPE)

IT **Etching**
(of silicon with hydrogen fluoride, hydrogen passivation from)

IT Vapor deposition **processes**
(app., for **silicon** for **silicon wafer processing**)

IT Epitaxy
(vapor-phase, of **silicon** for single-**wafer** processing)

IT 7664-39-3, Hydrogen fluoride (hydrofluoride), reactions
(**etching** of silicon by, hydrogen passivation from)

L88 ANSWER 13 OF 13 HCA COPYRIGHT 2003 ACS on STN
84:188549 Removal of silicon deposits on semiconductor processing apparatus. Muraoka, Hisashi; Asano, Masafumi; Ohhashi, Taizo (Tokyo Shibaura Electric Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 50158279 19751222 Showa, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1974-65053 19740610.
AB Si powder or amorphous Si deposited on a SiO2-based app. such as a **quartz boat** used for the processing of semiconductors is removed easily by using aq. 0.01-20 wt. % tetralkylammonium hydroxide solns. The soln. removes Si rapidly, but **etching** of SiO2 is very slow; the soln. is also capable of removing greases. Further, the tetralkylammonium hydroxides decomp. into volatile alcs. and amines upon heating and hence do not introduce addnl. impurities on the app. surface. Thus, a **quartz boat** used for impurity diffusion into Si semiconductors was immersed 15 min in aq. 0.05% Me4NOH soln. at 70.degree.: the Si powder and amorphous Si deposits on the **boat** were completely removed.
IC H01L
CC 76-13 (Electric Phenomena)
ST semiconductor processing app cleaning; **silicon** removal semiconductor **processing** app; tetramethylammonium hydroxide silicon removal
IT **Etching**
(of **silicon**, from silica **surfaces** by tetraalkylammonium hydroxide solns.)
IT 75-59-2
(cleaning agent, in removal of amorphous and powdered **silicon** from silica **surfaces**)

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L104 474 S CURV?(2A)L73
L105 7 S L104 AND L44

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L105 ANSWER 1 OF 7 HCA COPYRIGHT 2003 ACS on STN
TI Apparatus for catalytic deodorization of vent gases from kitchen garbage treatment machines

L105 ANSWER 2 OF 7 HCA COPYRIGHT 2003 ACS on STN
TI Tribocorrosion of stainless steels

L105 ANSWER 3 OF 7 HCA COPYRIGHT 2003 ACS on STN
TI Study of nonlinear luminescence-dose growth curves for the estimation of paleodose in luminescence dating results of Monte Carlo simulations

L105 ANSWER 4 OF 7 HCA
TI Application of a resistance heater to the MOCVD (Metal-Organic Chemical Vapor Deposition) growth of undoped and selenium-doped gallium arsenide

L105 ANSWER 5 OF 7 HCA
TI Application possibilities for reflection photometry in quantitative analysis

L105 ANSWER 6 OF 7 HCA
TI Dislocation scattering in silicon-on-insulator films

L105 ANSWER 7 OF 7 HCA
TI Nature of the luminescence of the lamellate phosphor $CdI_2.PbI_2$